Schedule: Tuesday 8th and 9th period 3:00 – 4:55 pm, NEB 101
Thursday 9th period 4:05 – 4:55, NEB 101
Thursday 10th period 5:10 – 6, MAEB 211

Instructor: Ann Gordon-Ross (ann@ece.ufl.edu)
Benton 319 - Office Hours: TBA and by appointment

TA: Scott Arnold (scottarnold@ufl.edu)
Office hours: TBA

Text: ”Computer Organization & Design", Patterson & Hennessy, Morgan-Kaufmann,
Revised 4th edition, ISBN-13 978-0123747501 (The green one only)

Web page: Available on Sakai

Topics Covered: Fundamentals in design and quantitative analysis of modern computer architectures and
systems, including instruction set architecture, basic and advanced pipelining, superscalar and VLIW
instruction-level parallelism, memory hierarchy, storage, and interconnects.

Prerequisites: EEL3701C and EEL 4712: Combinational and sequential logic design principles, advanced
modular design logic, finite state machines, and binary logic. Competence in programming with a hardware
description language (VHDL or Verilog) is required.

Lab Assignments: Assignments consisting of questions covering the material discussed in class and design
laboratories will be posted on the web and announced in class. There will be approximately 6 assignments.
These laboratories consist of coding a MIPS assembler/disassembler and designs implemented in VHDL,
increasing in complexity throughout the semester and building up to the design of a RISC 32-bit pipelined
microprocessor that implements a subset of the MIPS instruction set. Laboratories will also involve the use
of computer architecture simulators. The intent of the assignments is to increase the student's experience in
creating, implementing, and testing complex designs.

Homework Problems: There will be approximately 4 homework problem assignments consisting of
questions from the textbook. These questions are selected to reinforce course material and prepare students
for exam questions.

Lab Assignment and Homework Problem Submissions: All assignment reports will be submitted via
Sakai in PDF format. This means you will need to either prepare these submissions electronically or scan
your handwritten submissions for electronic submission. Physical paper submissions will not be accepted.
Late assignments will not be accepted! Please refer to the class policies document for additional
information on academic honesty policies.

Computer usage: You will use Quartus for the laboratories and VHDL designs, and a Web-accessible
portal to access computers architecture simulators. Detailed instructions will be given in an assignment.

Exams: There will be two midterm exams: the first one about half way through the semester and the
second one on the last day of class.

Grade: The grade will be calculated by the following weights:
  Assignments - 55%
  Homeworks – 10%
  Midterm 1 – 15%
  Midterm 2 – 20%
Final letter grade assignments will be determined based on the standard 90/80/70/60 break down with +/- grades assigned for the upper/lower 2.5%, respectively. Refer to this site for University grading policies: [http://www.registrar.ufl.edu/catalog/policies/regulationgrades.html](http://www.registrar.ufl.edu/catalog/policies/regulationgrades.html)

**Approximate Course Outline:** Refer to the course calendar for details (subject to change): *Note: since the lab structure of this semester’s offering is changing, this schedule is not accurate at the time of posting and will be changed throughout the semester, however, all topics listed will be covered at some point during the semester, only the ordering will change.*

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<td>Week 2:</td>
<td>Instruction set architecture design and hardware/software interface.</td>
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<td>Weeks 3-5:</td>
<td>Organization of single- and multi-cycle RISC microprocessors. Datapath and control logic. Introduction to the design of key datapath components (ALU, registers, shifters, signextenders) using VHDL behavioral and structural descriptions. Micro-programming.</td>
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<td>Week 6:</td>
<td>Performance: measurement, metrics, summarization and interpretation.</td>
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<td>Week 7:</td>
<td>Number systems: representation and operations; fixed and floating-point implementations.</td>
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<td>Week 12:</td>
<td>Virtual memory: address translation, placement, look-aside buffers.</td>
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<td>Week 15:</td>
<td>Advanced topics.</td>
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<td><strong>Throughout the semester:</strong></td>
<td>Guest speakers, company representatives, etc.</td>
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