Name: Mark Tyndall

Student ID: 3246 9206

EEL 4713: Computer Architecture - Spring 2012
Midterm 1 - 100 points possible

1. (12 pts) What are three drawbacks for taking a single cycle to execute each instruction?

~~8~~ 4

- A single cycle is as long as the slowest instruction
- Has two memories a instruction memory and a data memory
- /

Why is this a drawback?

Modern processors have separate caches

2. (6 pts) If you were to add a no-op instruction (the instruction performs no operation) to the MIPS ISA and considering the multi-cycle datapath, how many cycles would this instruction require?

NOP = AND $rd, $rd, $zero

10

2 cycles. One to load from memory. One to decode and set the select line so that no data passes through the system

3. (5 pts) Which of the following statements are potential arguments for MIPS to have 32 general-purpose registers (GPRs) $r0-$r31 instead of 64 GPRs? Mark all that apply.

2

1) The ALU can be made smaller with 32 GPRs
(2) The register file can be faster with 32 GPRs
3) The use of a 32-bit architecture implies the use of 32 GPRs
(4) Encoding of R-type instructions with 64 GPRs would lead to very few opcodes available in the 32-bit instruction word
(5) The control logic is simpler with 32 GPRs

4. (10 pts) The MIPS "jump and link" instruction implicitly stores the PC+4 value to a fixed register (R31). Discuss the implications, if any, if the ISA was changed such that any arbitrary register could be specified.

10

If register was specified then there would be less bits available for addresses, thus making your jump page smaller and would also mess up the idea of aligning the bits for the PC's adder.

5. (7 pts) Which method, callee or caller saved registers, may result in fewer assembly instructions and why.

6.5 Using the callee saved register will result in few instructions. If the caller is using the temp regs ($t0 to $t7), the caller must save them to the stack before doing call. otherwise only the callee has to save the save regs ($s0 - $s7) to the stack. only the ones the callee uses

6. (10 pts) In MIPS ISA the source registers are fixed (*$rs* and *$rt*), while the destination register can be *$rd* (R-type) or *$rt* (I-type). Why is this approach preferable to keeping the destination register fixed and the source registers different?

0 R-Types require three arguments to the opcodes while I-Types require two and an immediate value from memory. So only only $Rd or $Rt are ever destination registers.

This is just info about the inst format. You didn't answer the question

7. (50 pts total) Consider the addition of a new instruction into the MIPS instruction set given the multi-cycle instruction execution implementation. This instruction, *inc2 $rd, $rt*, is used to automatically increment the values stored in both registers *$rd* and *$rt* in a single instruction (i.e., *$rd* = *$rd* + 1 and *$rt* = *$rt* + 1).

21 Pretty sure I did this as $RS and $RT I did account for writing to $Rd first

a) (10 pts) Discuss why this instruction cannot be supported by the current multi-cycle datapath?

2 how is this an issue?

The output of the ALU is only 32-bits. This would require no a 64-bit output and bus. Also the register file only has one 32-bit write port.

The controller would also need to be modified for the R-Type instruction. ?

how ?

why ?

49.5/100

b) (15 pts) If the instruction cannot be supported by the current multi-cycle datapath, discuss the architectural and control logic changes, at a high level, that are necessary to support this instruction.

- The R-Type state path would need to be modified for this special case. (Main Controller) how? why?
- The bus width from the ALU to Register File would need to be increased to 64-bits why?
- The register file will need an additional write port, additional write address lines — Yes
- The ALU needs to be modified to handle the new instruction — yes but how? why?
- The ALU decoder needs to decode the new data in function field and Op Code.

d) (15 pts) How many cycles will this new instruction require? What will be done on each cycle?

3

3 cycles
1. Decode. Set proper select lines
2. Set Reiste destination
3. Store data to registe file

ALU ops currently take 4 cycles, So how is yours faster than that?

e) (5 pts) Does the clock cycle time need to change to support this new instruction?

5

No

f) (5 pts) What instruction type (I-, R-, J-type) would be most appropriate for this instruction and why?

5

R-Type. The instruction doesn't require any memory accesses. The data is already in the registe file.