EEL 4713C – Computer Architecture
Syllabus – Spring 2012

Schedule: Tuesday 8th and 9th period 3:00 – 4:55 pm, CHE 316
Thursday 9th period 4:05 – 4:55, CHE 316
Thursday 10th period 5:10 – 6, CHE 316

Instructor: Ann Gordon-Ross (ann@ece.ufl.edu)
LAR 221 - Office Hours: TBA and by appointment

TA: Scott Arnold (scottsarnold@ufl.edu)
Office hours: TBA

Text: "Computer Organization & Design", Patterson & Hennessy, Morgan-Kaufmann, Revised 4th edition, ISBN-13 978-0123747501

Web page: Available on Sakai

Topics Covered: Fundamentals in design and quantitative analysis of modern computer architectures and systems, including instruction set architecture, basic and advanced pipelining, superscalar and VLIW instruction-level parallelism, memory hierarchy, storage, and interconnects.

Prerequisites: EEL3701C. Combinational and sequential logic design principles. Competence in programming with a hardware description language (VHDL or Verilog) is required.

Assignments: Assignments consisting of questions covering the material discussed in class and design laboratories will be posted on the web and announced in class. There will be approximately 7 assignments. These laboratories consist of designs implemented in VHDL, increasing in complexity throughout the semester and building up to the design of a RISC 32-bit pipelined microprocessor that implements a subset of the MIPS instruction set. Laboratories will also involve the use of computer architecture simulators. The intent of the assignments is to increase the student's experience in creating, implementing, and testing complex designs.

Homework: There will be 4 homework assignments consisting of questions from the textbook. These questions are selected to reinforce course material and prepare students for exam questions.

Assignment submissions: All assignment reports will be submitted via Sakai. This means you will need to either prepare these submissions electronically or scan your handwritten submissions for electronic submission. ***Late assignments will not be accepted!*** Please refer to the class policies document for additional information on academic honesty policies.

Computer usage: You will use Quartus for the laboratories and VHDL designs, and a Web-accessible portal to access computers architecture simulators. Detailed instructions will be given in assignment 1.

Exams: There will be two midterm exams: the first one about half way through the semester and the second one on the last day of class.

Grade: The grade will be calculated by the following weights:
Assignments - 50%
Midterm 1 – 25%
Midterm 2 – 25%
Final letter grade assignments will be determined based on the standard 90/80/70/60 break down with +/- grades assigned for the upper/lower 2.5%, respectively Refer to this site for University grading policies: http://www.registrar.ufl.edu/catalog/policies/regulationgrades.html

Approximate Course Outline: Refer to the course calendar for details (subject to change)

Weeks 0-1:	Introduction. Components of a computer system. Evolution of technology.
Week 2:	Instruction set architecture design and hardware/software interface.
Weeks 3-5:	Organization of single- and multi-cycle RISC microprocessors. Datapath and control logic. Introduction to the design of key datapath components (ALU, registers, shifters, signextenders) using VHDL behavioral and structural descriptions. Micro-programming.
Week 6:	Performance: measurement, metrics, summarization and interpretation.
Week 7:	Number systems: representation and operations; fixed and floating-point implementations.
Weeks 8-9:	Pipelining. Data hazards and forwarding. Superscalar design.
Weeks 10-11:	Memory hierarchies, caches: organization, implementation and performance.
Week 12:	Virtual memory: address translation, placement, look-aside buffers.
Weeks 13-14:	Input/output. Disk technologies, busses and protocols. I/O system design. Redundant arrays of inexpensive disks (RAID).
Week 15:	Advanced topics.