EEL4713 Assignment #5
Fall 2014
Final Demo: Scheduled with TA before 12/11/14 @ 8 PM
Report Due: Saturday 12/13/14 @ 11:55pm Via Sakai
Developed by Scott Arnold and Ann Gordon-Ross Fall 2012

Overview;
In this assignment, you will be modifying your multi-cycle implementation of a MIPS processor to include hazard detection. Your processor will need to be able to successfully execute Lab5.mif (provided in assignment 2) in the same way that it did in the previous lab, you should get the same content in your registers and memory block. You will use Lab5.mif to demonstrate the functionality of your processor for the in-lab demo. Note: If you are still having errors in your multi-cycle processor without hazard detection, you must fix those errors before this assignment can be successfully completed.

In this assignment, you will perform the following tasks:

DEMOS: final demo of working processor
2.1: Design and simulate a MIPS multi-cycle processor
2.2: Annotate the simulations for the Lab5.mif demo program
3: Review deliverables and write the report

Section 1: Setup
There is no setup in this assignment.

Section 2: Laboratory
2.1: Multi-Cycle Processor
In this assignment, you will be modifying your pipelined multi-cycle processor from Assignment 5 to include hazard detection and forwarding logic. Your processor will have to successfully execute the 29 instructions listed on the front of the green reference sheet.

Use your hazard table from assignment 4 to establish your hazards. If your table was incomplete or incorrect, you may use the hazard table provided with this assignment (note that this file will be distributed via Sakai after the assignment 4 due date).

At this point your processor should be able to execute code with all the different hazards listed in the hazard table without any problems.

2.2: In-Lab DEMOS
Final Demo: Demonstrate the functionality of your processor using the Lab5.mif file

Include a section in your report where you annotate the functional simulation output of your processor running the program.

Timing analysis of your processor should be done with the **Cyclone IV Gx - EP4CGX150DF3117** FPGA as your target device. Part of your demo grade will be based on the maximum clock rate listed in the timing analyzer report. Frequencies above 45MHz will receive extra credit. Anything below 25MHz will receive a zero for the final demo.

Section 3: Report
Each of the remaining assignments should follow this format:

1. The report should contain the following sections
   - Cover page – with your name, date, and assignment number
   - Introduction – briefly comment on the assignment and what it accomplishes
   - Lab5 Demo Program:
     - Annotated simulation of the output of your processor from the Lab5.mif file used in the final demo.

- Appendix

2. The report needs to be typed. Annotations should not be scans of hand-drawn annotations and illegible annotations are almost as bad as no annotations.
3. Any waveform that is not labeled and annotated will not be considered as valid.
4. Make sure you use the names for inputs, outputs, and entities as outlined in the assignment. This will be essential for connecting these components together in later assignments.

Grade Breakdown

Section	**Deliverables**	**Percentage of Total grade**
Final Demo	Your processor running the Lab5.mif file demonstrated to be working	20%
2.1	Design of your multi-cycle processor with detailed diagrams	20%
2.2	Lab5.mif decode, similar to previous lab	55%
Report	Report follows the format given in section 3 (3%). Report is neat and professional (2%).	5%