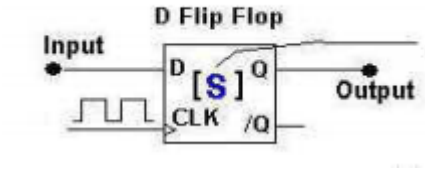
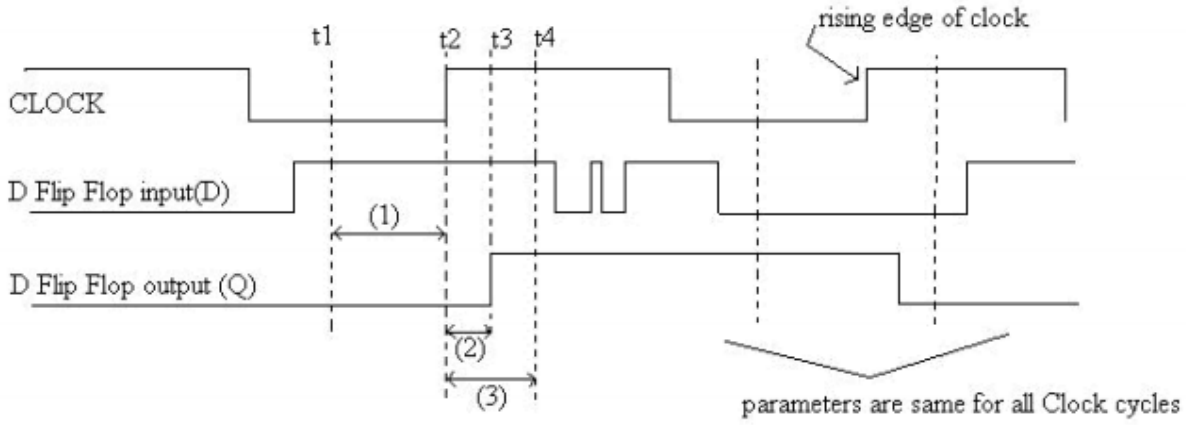
Propagation Delays:

Propagation delay (PD) for the circuit can be calculated as the summation of all delays encountered from where the clock occurs to the output.

Propagation delay is the time required for the output to reach from 10% to 90% of its final output level when the input changes. Calculate from your wave forms. Example of a Data Flip-Flop shown below.





(1) i.e. [t2 - t1] is the Setup Time: the amount of time Input is held constant BEFORE the clock tick.

(2) i.e. [t3 - t2] is the Propagation delay of the Flip Flop: the time for the input to propagate and influence the output.

(3) i.e. [t4 - t2] is the Hold time: the amount of time the Input is held constant AFTER the clock tick.

(The above timing diagram has 2 clock cycles; the timing parameters for the second cycle will also be similar to that of the first cycle)

Maximum clock rate:

Maximum clock rate is calculated using the formulae

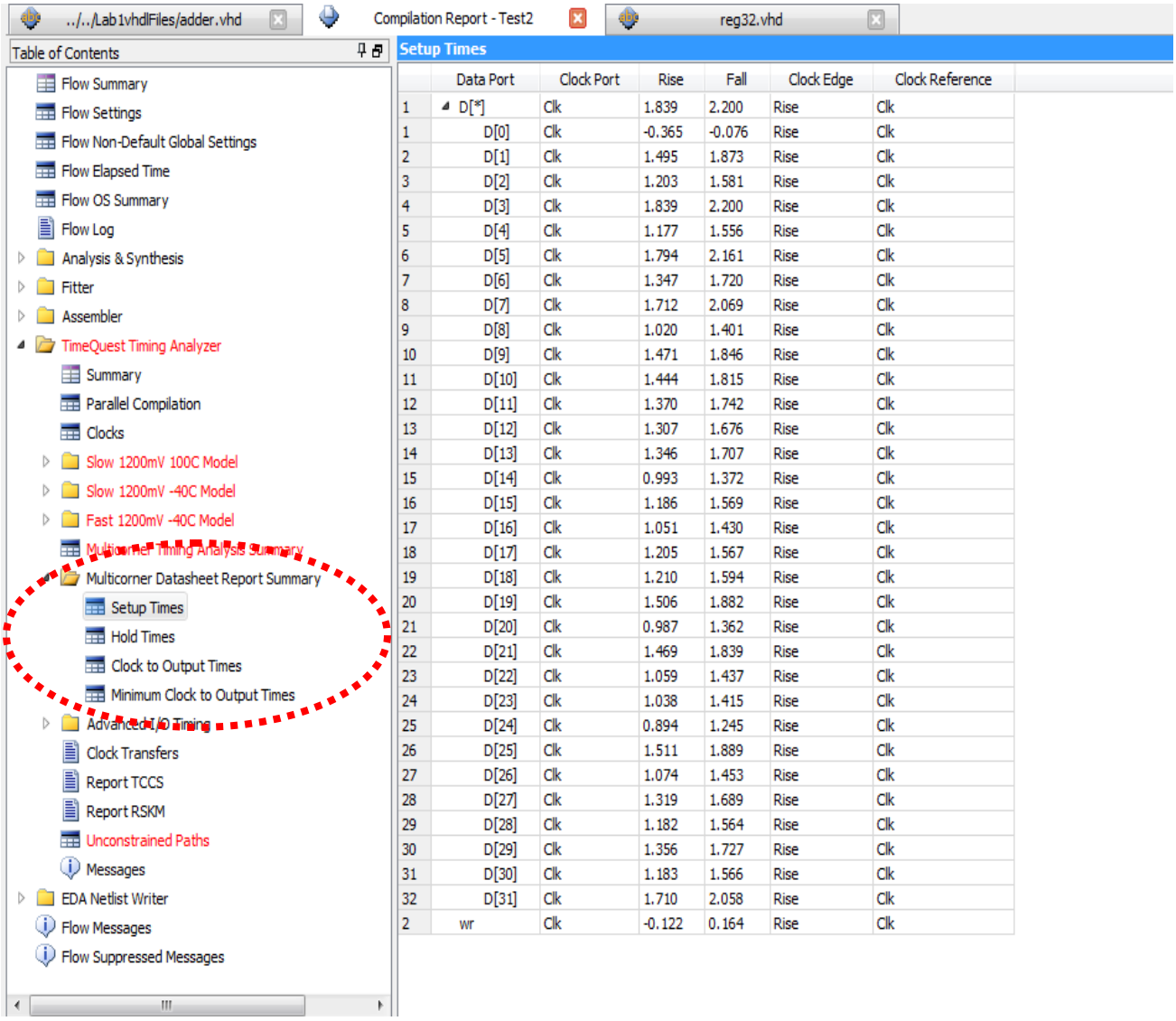
MCLK = 1/ TMIN

So we will have to calculate TMIN first. TMIN here refers to the minimum time period for correct operation of the circuit, so it is calculated using all worst cases (maximum delays).

Other useful things:

You can also calculate these delays using time quest multicorner timing and timing model datasheet reports.

Following link shows description of what each report shows plus what each row/column in the report signifies
http://quartushelp.altera.com/13.0/mergedProjects/report/rpt/rpt_file_multicorner_timing.htm



	Data Port	Clock Port	Rise	Fall	Clock Edge	Clock Reference
1	D[*]	Clk	1.839	2.200	Rise	Clk
1	D[0]	Clk	-0.365	-0.076	Rise	Clk
2	D[1]	Clk	1.495	1.873	Rise	Clk
3	D[2]	Clk	1.203	1.581	Rise	Clk
4	D[3]	Clk	1.839	2.200	Rise	Clk
5	D[4]	Clk	1.177	1.556	Rise	Clk
6	D[5]	Clk	1.794	2.161	Rise	Clk
7	D[6]	Clk	1.347	1.720	Rise	Clk
8	D[7]	Clk	1.712	2.069	Rise	Clk
9	D[8]	Clk	1.020	1.401	Rise	Clk
10	D[9]	Clk	1.471	1.846	Rise	Clk
11	D[10]	Clk	1.444	1.815	Rise	Clk
12	D[11]	Clk	1.370	1.742	Rise	Clk
13	D[12]	Clk	1.307	1.676	Rise	Clk
14	D[13]	Clk	1.346	1.707	Rise	Clk
15	D[14]	Clk	0.993	1.372	Rise	Clk
16	D[15]	Clk	1.186	1.569	Rise	Clk
17	D[16]	Clk	1.051	1.430	Rise	Clk
18	D[17]	Clk	1.205	1.567	Rise	Clk
19	D[18]	Clk	1.210	1.594	Rise	Clk
20	D[19]	Clk	1.506	1.882	Rise	Clk
21	D[20]	Clk	0.987	1.362	Rise	Clk
22	D[21]	Clk	1.469	1.839	Rise	Clk
23	D[22]	Clk	1.059	1.437	Rise	Clk
24	D[23]	Clk	1.038	1.415	Rise	Clk
25	D[24]	Clk	0.894	1.245	Rise	Clk
26	D[25]	Clk	1.511	1.889	Rise	Clk
27	D[26]	Clk	1.074	1.453	Rise	Clk
28	D[27]	Clk	1.319	1.689	Rise	Clk
29	D[28]	Clk	1.182	1.564	Rise	Clk
30	D[29]	Clk	1.356	1.727	Rise	Clk
31	D[30]	Clk	1.183	1.566	Rise	Clk
32	D[31]	Clk	1.710	2.058	Rise	Clk
2	wr	Clk	-0.122	0.164	Rise	Clk