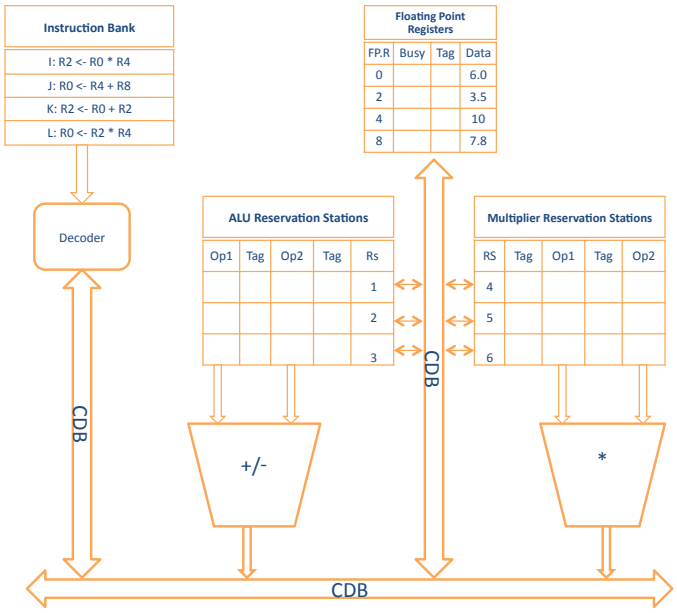
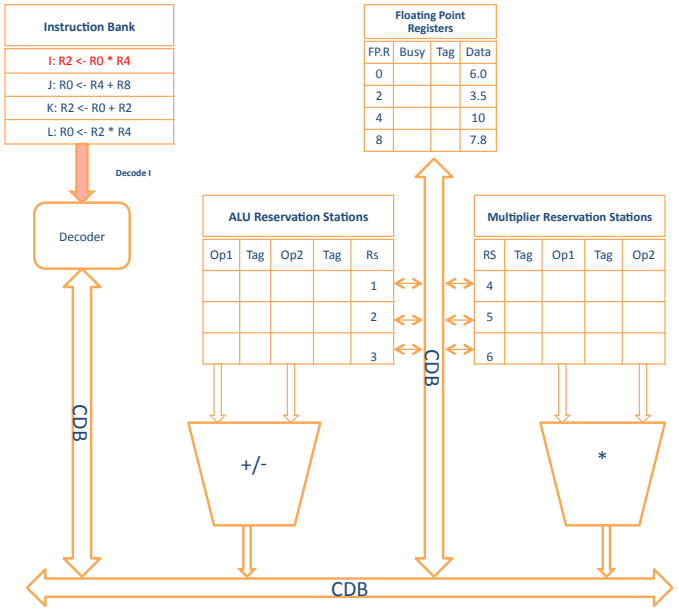
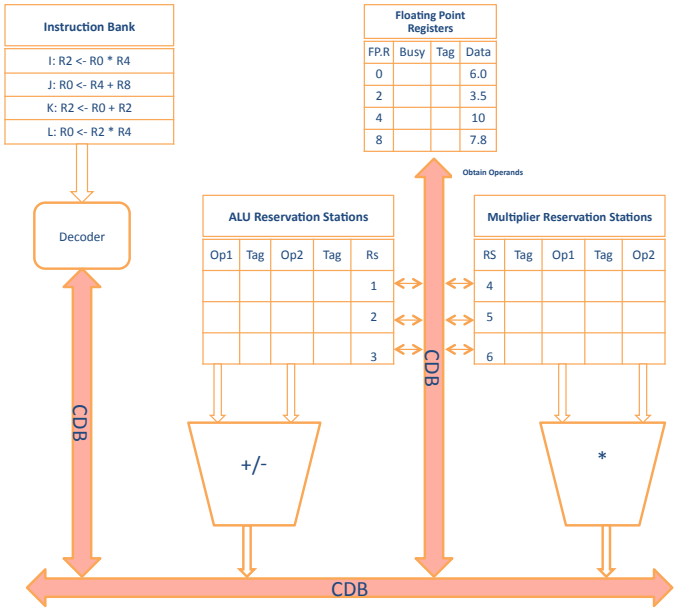
Assumptions

- One instruction can be fetched at each cycle.
- Latency is 2 cycles for ALU, and 3 for multiplier
- Instructions begin execution once fetched
- In case two instructions finish at the same cycle, both can commit on the same cycle and the CDB arbitrates who writes first



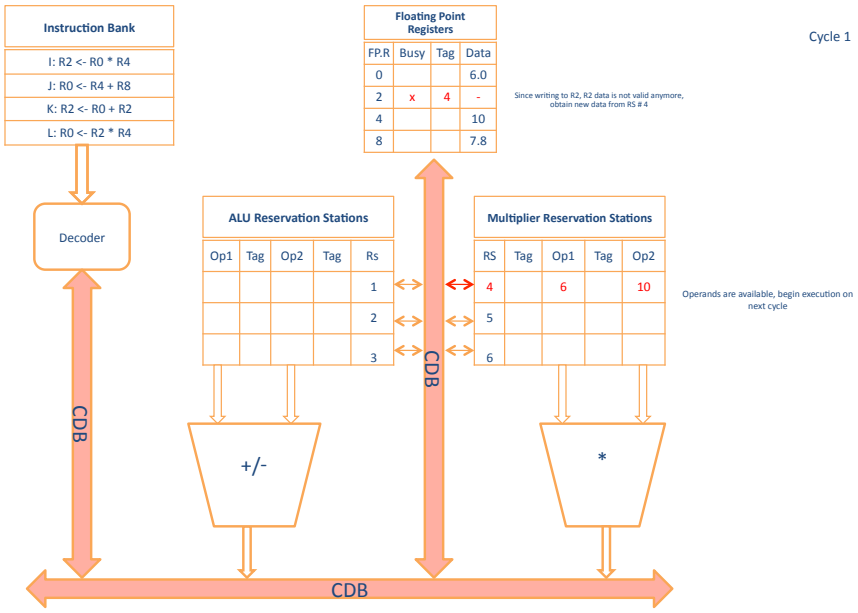


Cycle 1

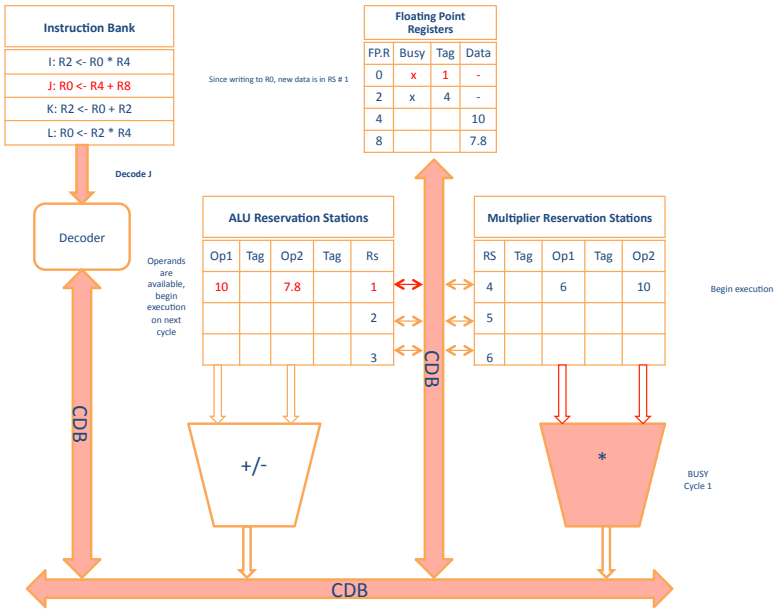


Cycle 1

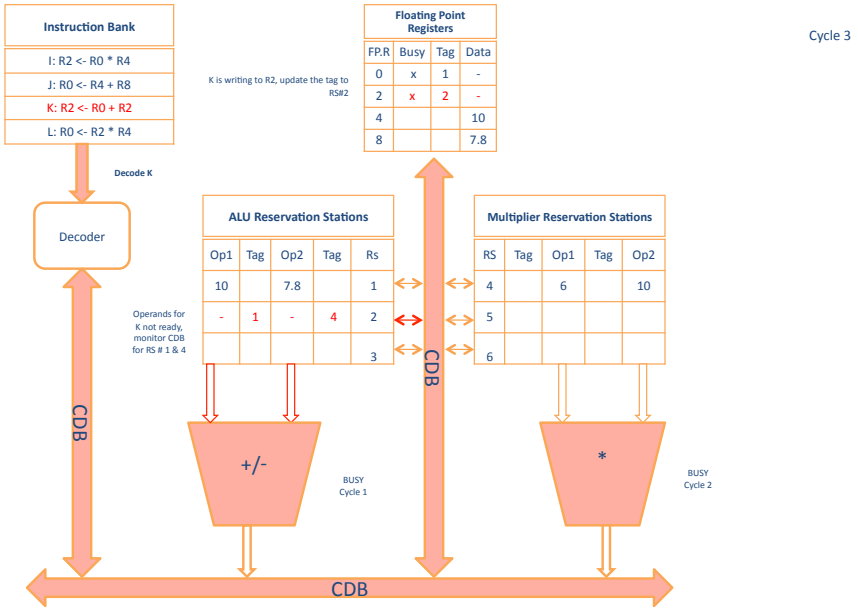
Cycle 1



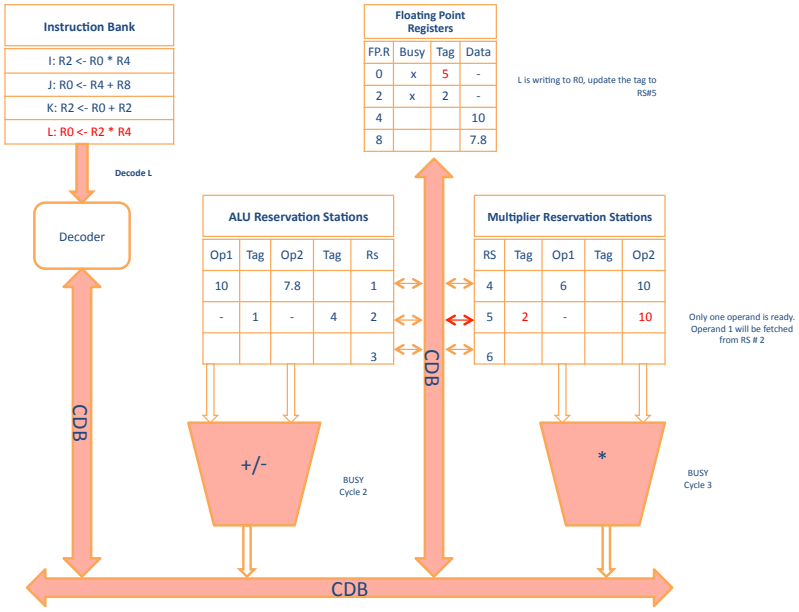
Cycle 2

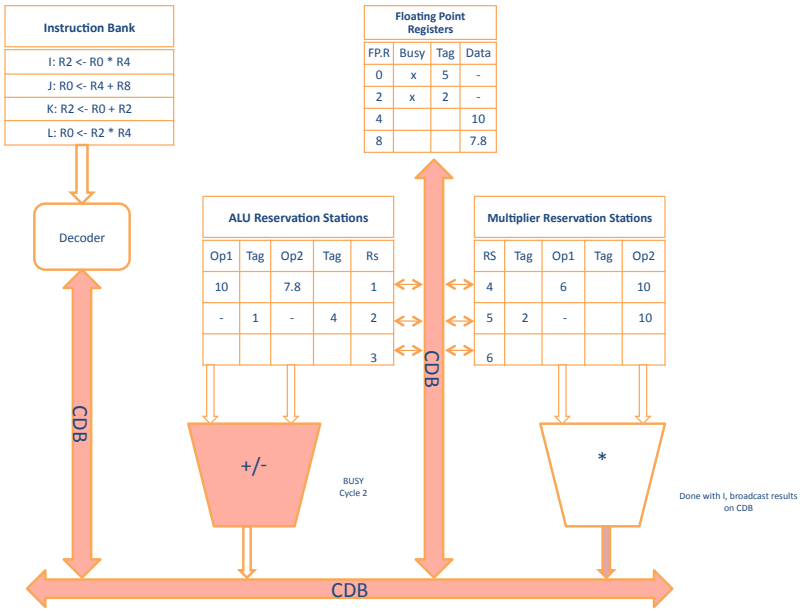


Cycle 3

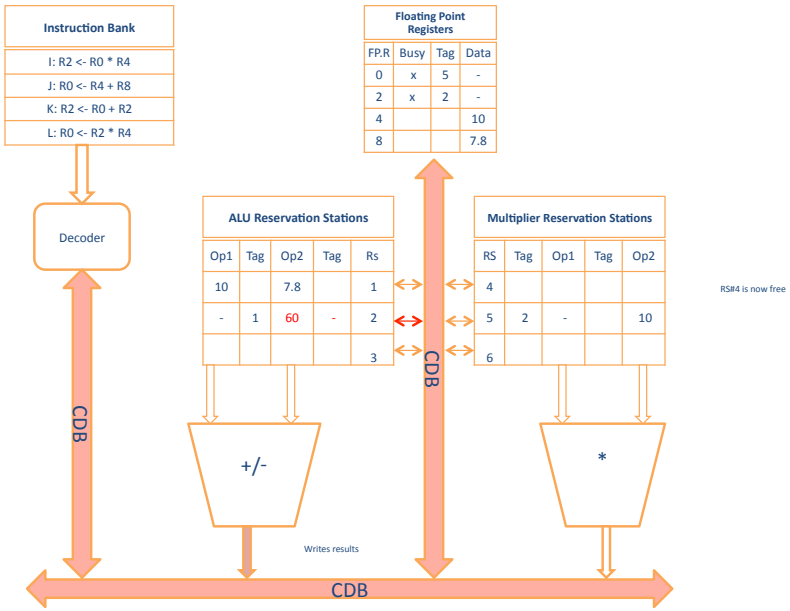


Cycle 4



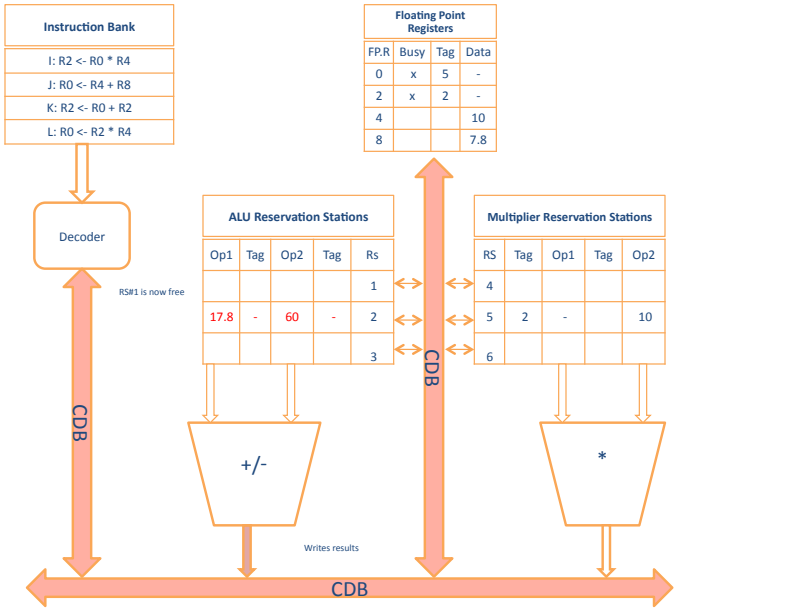


Cycle 5

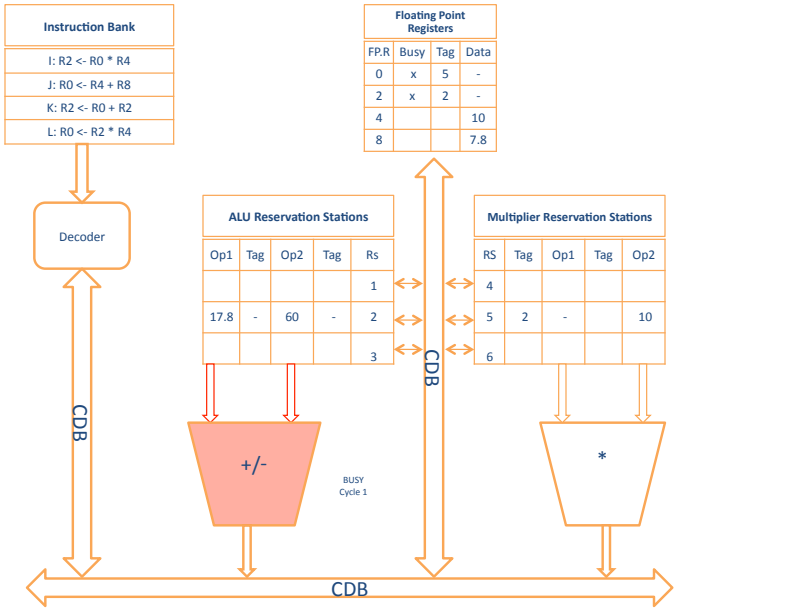


Cycle 5

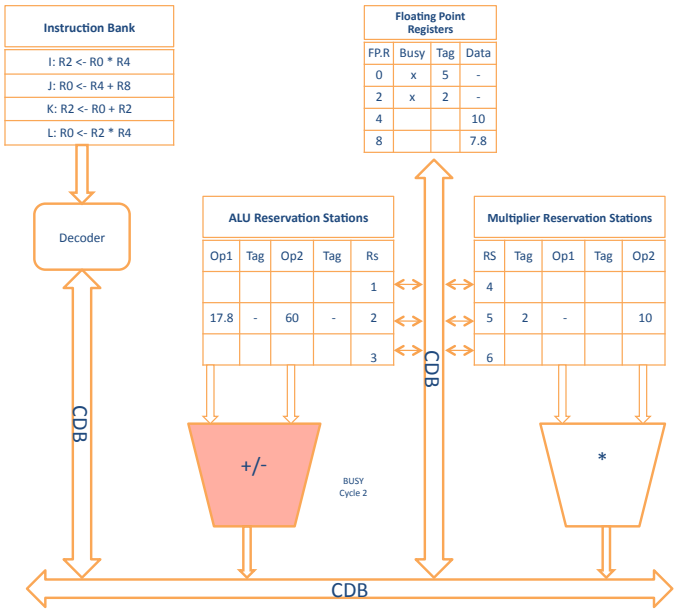
RS#4 is now free



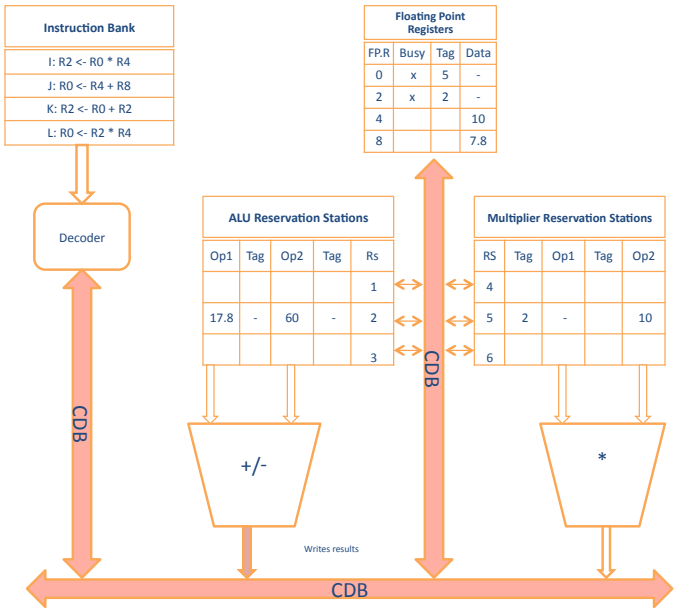
Cycle 5



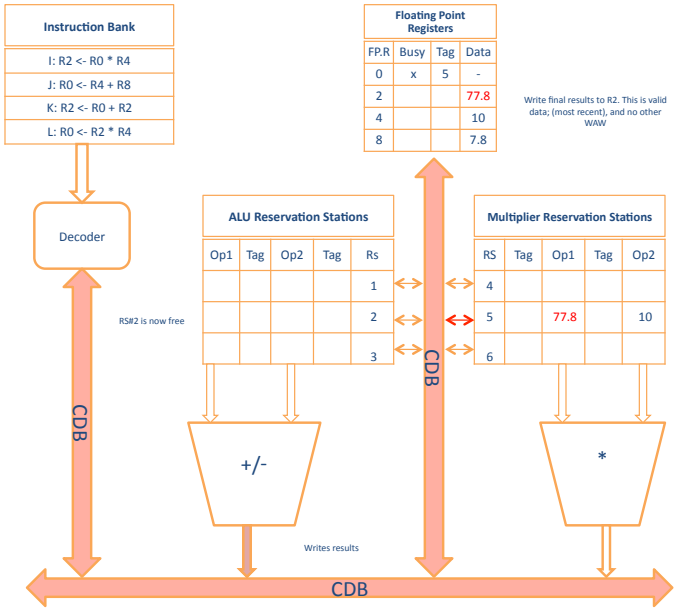
Cycle 6



Cycle 7



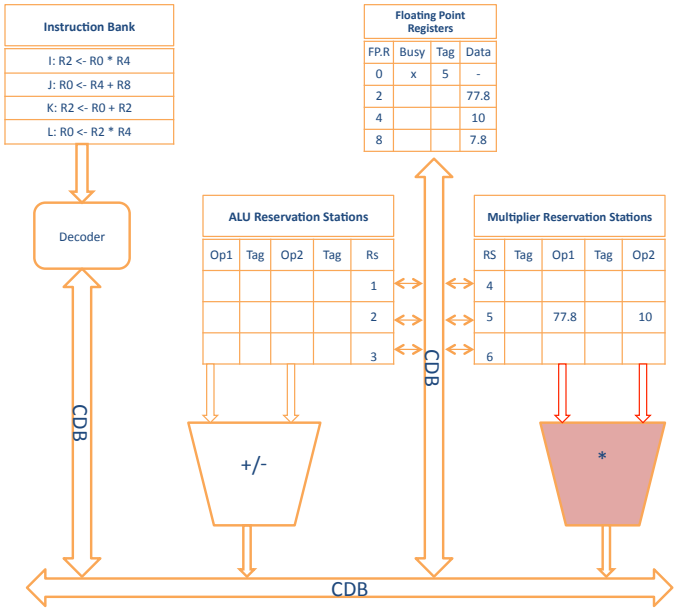
Cycle 8



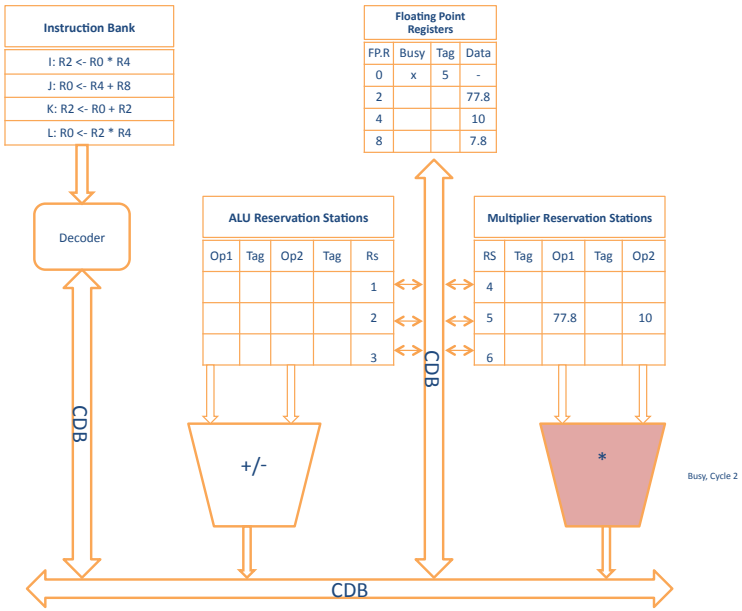
Cycle 8

Write final results to R2. This is valid data; (most recent), and no other WAW

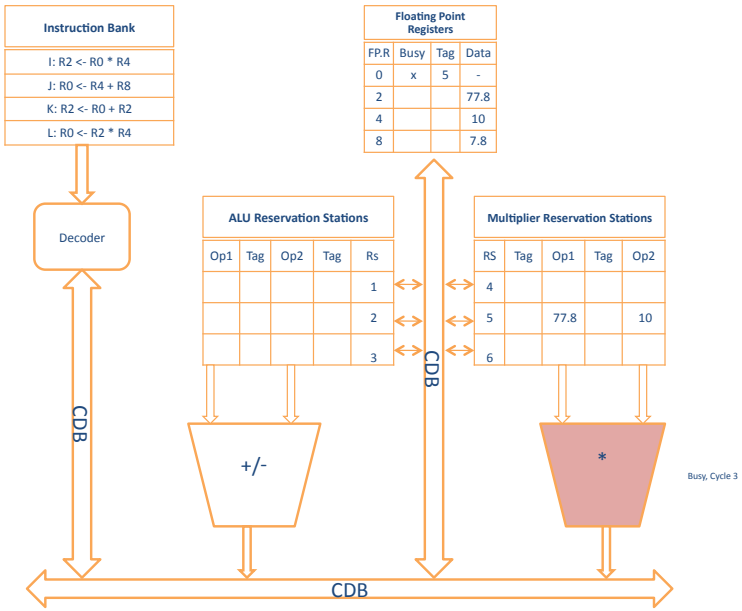
RS 5, observes a write it has been looking for on the CDB (77.8). Now Multiplier can begin execution on cycle 9



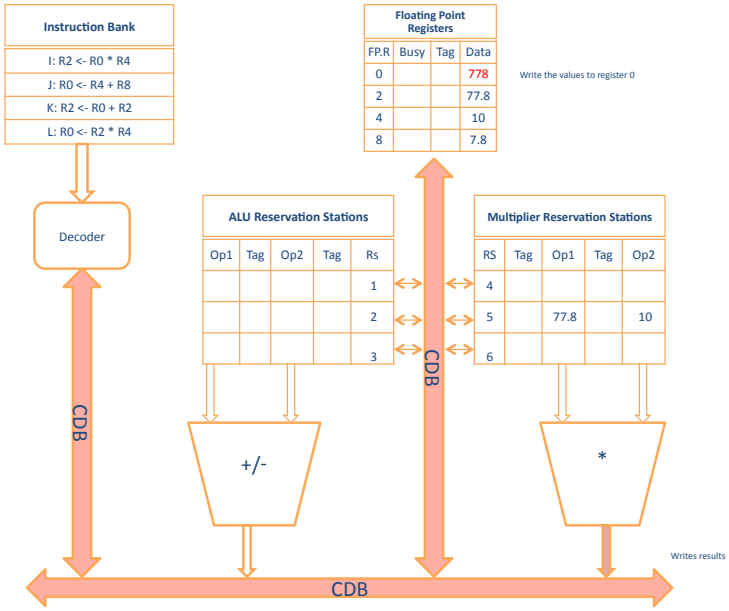
Cycle 9



Cycle 10



Cycle 11



Cycle 11