A Near-Threshold, 0.16 nJ/b OOK-Transmitter With 0.18 nJ/b Noise-Cancelling Super-Regenerative Receiver for the Medical Implant Communications Service

Chao Ma, *Member, IEEE*, Changhui Hu, *Member, IEEE*, Jiao Cheng, *Student Member, IEEE*, Lingli Xia, and Patrick Yin Chiang, *Member, IEEE*

***Abstract*—A 0.16 nJ/b MICS transmitter and 0.18 nJ/b super-regenerative receiver are demonstrated, where each is specifically designed to operate in the near-threshold region. The low-VDD transmitter utilizes a sub-harmonic injection-locked ring oscillator, edge combiner for frequency multiplication, and class-C power amplifier. The low-VDD receiver introduces a replica super-regenerative receiver as a method to reject common-mode noise sources, such as supply/substrate coupling, thereby reducing undesired self-oscillations and improving BER. Designed in a 90-nm CMOS process, the test-chip measurements show a sensitivity of -80 dBm at 500 kb/s and -65 dBm at 1 Mb/s, respectively, at a BER less than 10^{-3}, with 340 μW total power.**

***Index Terms*—Low power, low voltage, MICS, near-threshold, on-chip noise immunity, pre-distorting linearization, sub-harmonic injection locking, super-regenerative receiver, wireless body area network (WBAN).**

I. Introduction

POWER consumption is one of the most critical requirements for future wireless body-area network (WBAN) sensors [1]–[3]. Future biosensing system-on-chips (SoCs) may contain a wide variety of circuit components, including the electrophysiology sensor interface, analog-to-digital converter, digital signal processor, microprocessor, power management, and wireless interface. Of these components, the wireless transceiver is typically the dominant consumer of power. Recent papers have reported that wireless transceiver power can consume between 70–80% of the total system power [4], [5]. Because there are many design considerations for the wireless transceiver, such as duty-cycling, modulation scheme, frequency plan, circuit design, input sensitivity, and antenna size, the development of an energy-efficient WBAN radio is extremely challenging.

In addition to power consumption, reliability and noise immunity are key requirements for next-generation BAN radios. As the radio will be placed in various locations around the body, severe multipath [6], [7], body absorption and movement artifacts can affect the signal-to-noise ratio of the radio transceiver. Furthermore, due to system-on-chip (SoC) integration with other noisy blocks, such as the processor, ADC, and switching power supply, significant noise will be introduced into the sensitive RX through supply or substrate coupling, resulting in degraded bit-error rate. This problem is especially critical for high-gain OOK-based super-regenerative receivers, which have difficulty discerning between coupling noises and the small-signal data input [8].

After the FCC released the medical-implant communication system (MICS) [9] standard operating in 402–405 MHz band in 1999, the design of the MICS radio has been a very attractive research area. A 2.9 nJ/b MSK transmitter and 3.3 nJ/b OOK super-regenerative receiver was reported in [10]. A FSK transceiver with good interference immunity was presented in [11], adopting a Q-enhancement low-IF receiver and direct-modulation transmitter to satisfy requirements for high selectivity and low energy consumption. In [12], a highly integrated 0.45 nJ/b FSK transmitter with 20% global efficiency was presented by utilizing cascaded multiphase direct injection-locking for frequency multiplication. While these previously demonstrated radios proposed several new techniques to achieve low-power consumption, issues related to noise coupling and low-VDD operation have remained unaddressed.

In this work, we introduce a MICS (402–405 MHz) transceiver that achieves improved energy-per-bit by operating the TX/RX in the near-threshold domain ($\mathrm{VDD} \sim 0.65$ V). Operation of the radio in the near-threshold domain is critical, as previously reported, micro-powered systems have shown substantial improvements in energy-efficiency by operating in low-VDD [13]–[15]. In addition, we address the problem of undesired sensitivity to external noise by utilizing a replica super-regenerative

Manuscript received July 25, 2012; revised December 18, 2012; accepted February 16, 2013. Date of publication June 04, 2013; date of current version January 28, 2014. This work was supported in part by the Catalyst Foundation, the National Science Foundation IIP-1127853, and the 1000-Talents Recruitment Program. This paper was recommended by Associate Editor Z. Wang.

C. Ma was with the School of Electrical Engineering and Computer Science, Oregon State University, Corvallis, OR 97331 USA. She is now with Marvell Technology Ltd., Shanghai 201203, China.

C. Hu was with Oregon State University, Corvallis, OR 97331 USA. He is now with Marvell Semiconductor, Santa Clara, CA 95054 USA.

J. Cheng and L. Xia are with the School of Electrical Engineering and Computer Science, Oregon State University, Corvallis, OR 97331 USA.

P. Y. Chiang is with the State Key Laboratory of ASIC and Systems, Fudan University, Shanghai 201203, China, and also with the School of Electrical Engineering and Computer Science, Oregon State University, Corvallis, OR 97331 USA (e-mail: pchiang@eecs.oregonstate.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TBCAS.2013.2253555

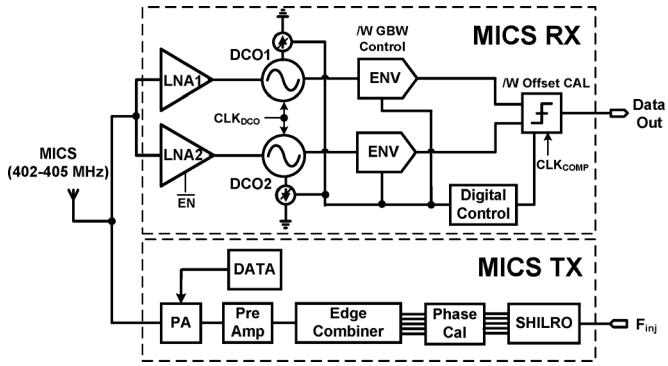


Fig. 1. Block diagram of the proposed MICS transceiver.

oscillator, making any supply/substrate noise injection appear common-mode, thereby improving bit-error rate.

The paper is organized as follows: Section II introduces the system architecture of the transceiver and key techniques in the design. Section III explains the design considerations of the sub-harmonic injection-locked ring oscillator while operating with a near-threshold supply voltage. Section IV explains the theory of super-regeneration and the proposed technique for improving noise immunity. Section V details the circuit implementations. Sections VI and VII show the measurement results of the transceiver and conclude the paper.

II. Transceiver Architecture Overview

Reducing the number of external components is an important factor for size-constrained medical applications, motivating the use of simplified, highly integrated architectures. Hence, a super-regenerative receiver using OOK (on-off keying) modulation is chosen due to its simplicity, high sensitivity, and low-power consumption [10]. The proposed MICS transceiver architecture is shown in Fig. 1. A received OOK signal is coupled into the super-regenerative receiver (SRR), which consists of a digitally-controlled oscillator (DCO) with a 1st-stage LNA. The DCO is quenched by the clock signal $\mathrm{CLK_{DCO}}$ and will startup earlier if a "1" is received. A replica SRR is introduced to mitigate the problem of on-chip noise coupling by generating a common-mode reference envelope to compare against. During normal operation, the replica LNA is disabled so that it rejects the input RF signal, while the replica DCO and envelope detector (ENV) are biased at the same operating conditions as the main signal chain. In the OOK modulated transmitter, a sub-harmonic injection-locked ring oscillator (SHILRO) operating at 80 MHz is locked to a 16 MHz off-chip input reference. Using the five equally spaced phases generated by the 5-stage ring oscillator, a 5x higher frequency (400 MHz) is obtained at the output of the proceeding edge combiner (EC). Static timing calibration using capacitively-tuned inverter buffers are added to the multiphase outputs of the SHILRO in order to trim any phase asymmetries. A pre-amplifier is added in front of the class-C power amplifier (PA) to insure adequate output drive, since the class-C PA requires large signal amplitude at its gate, due to its biasing in the cut-off region.

For the MICS standard [9], the minimum spectral specifications require a relatively relaxed frequency stability of 100 ppm. Hence, alternative frequency synthesis techniques other than the conventional phase-locked loop (PLL) can be employed. Among these alternative techniques, injection locking has attracted much attention recently [12], [16]. This technique can significantly suppress the phase noise of the ring oscillator, improve the energy-efficiency, and conveniently generate multiple time-interleaved phases for the proceeding edge combiner. However, the disadvantage may be increased reference spurs due to asymmetric injection.

For the MICS band, the transmitter output power is limited, as a maximum of -16 dBm equivalent isotropically radiated power (EIRP) is only allowed. Furthermore, inside the human body, the antenna gain is relatively low due to the small antenna size and any efficiency degradation due to human body interactions. Fortunately, MICS usage is intended for short-range applications, such that the path loss in free-space is limited. For example, the loss at 1 meter radius is -24.5 dB using $20\log_{10}(\lambda/4\pi\mathrm{d})$. With a -4 dBi on-body antenna gain and 30 dB path-loss from human tissue propagation [17], the receiver's sensitivity is required to be at least -74.5 dBm ($P_{\mathrm{sens}} \leq P_{\mathrm{tx}} + G_{\mathrm{ant}} + G_{\mathrm{path}}$). Additional requirements for this wireless medical application include selectivity and interferer rejection, high data rate, and a low power sleep-mode. The proposed SRR addresses all of the above requirements by incorporating low-voltage operation, heavy duty-cycling of the quench signal, fast oscillator start-up, Q-enhancement, and on-chip noise immunity. These design tradeoffs and specifics will be discussed in the following sections.

III. Near-Threshold Transmitter

The proposed MICS transmitter utilizes the technique of sub-harmonic injection locking and edge combining, eliminating the conventional frequency-multiplying PLL. This is advantageous, as a PLL is not only power hungry, but also exhibits a slow settling time, preventing the use of aggressive duty cycling that can help minimize static power.

A. Theory of Sub-Harmonic Injection Locking

The injection-locking phenomenon has been explored recently for frequency synthesis and phase lock [12], [16], [18]. When locked, an injection-locked system exhibits the same noise transfer function as a first-order PLL, tracking the low-frequency phase noise from the injected signal $\mathcal{L}_{\mathrm{inj}}$ and the high-frequency phase noise of the free-running oscillator $\mathcal{L}_{\mathrm{osc}}$, where the locking range ω_{L} is analogous to the PLL bandwidth. Sub-harmonic injection occurs when the incident frequency is a sub-harmonic of the oscillator free-running frequency ($\omega_{\mathrm{inj}} = \omega_0/\mathrm{N}$), such that the in-band phase noise is constrained to $\mathcal{L}_{\mathrm{inj}} + 20\log_{10} N$ [19], [20]. As the division ratio N increases, the noise rejection degrades accordingly, as corrections from the injected signal are too sparse to clean-up the oscillator.

Reference [16] previously developed an expression for the single-sided locking range of an n-stage ring oscillator, which predicts its noise shaping and settling behavior

$$\omega_L = \frac{k}{n\eta/\pi - k\cos\alpha}\frac{2\omega_0}{n\sin(2\pi/n)} \tag{1}$$

where ω_0 denotes the free running frequency of the ring oscillator, k denotes the injection strength, α is the phase difference between the resultant output of the ring oscillator and the injected input signal, and η is a proportionality constant with a value of approximately one. To apply (1) to this sub-harmonic injection-locked oscillator, the injection strength k should be divided by a factor of N since the injection occurs once every N cycles.

B. Near-Threshold Voltage Operation

For energy-constrained biomedical implants, reducing the supply voltage to near the threshold voltage is an effective technique to improve energy-efficiency while still maintaining adequate performance [21]. Dynamic power consumption is proportional to $V^2 f$, and thus is reduced quadratically as the supply voltage is decreased. However, problems such as constrained headroom, device variation, and leakage current become significant as the supply voltage approaches this near-threshold region. Any such non-idealities from near-threshold operation must therefore be analyzed in detail to guarantee robust operation at low-VDD.

Phase noise degradation of the injection-locked ring oscillator is one important factor that will limit the potential supply scaling. As the supply voltage decreases, the intrinsic thermal noise (kT/C), relative to the linear reduction in the capacitor voltage-swing, results in degraded signal-to-noise ratio and therefore larger oscillator phase noise. Furthermore, the slower inverter rise/fall edge rates degrade the impulse sensitivity function (ISF), resulting in higher phase noise [22].

Fig. 2 shows the simulated phase noise of the ring oscillator running at two operating conditions, both with their 5th sub-harmonics used as the input injection frequencies: VDD $=$ 1.0 V, $f_{\rm osc} = 400$ MHz; VDD $=$ 0.6 V, $f_{\rm osc} = 80$ MHz. These two cases are compared as the 400 MHz local oscillation frequency can be generated either directly by the 1 V-400 MHz-SHILRO with higher power consumption (case A), or by the 0.6 V-80 MHz-SHILRO with the edge combiner (case B). At 300 kHz offset, the injection-locked oscillator phase noise of case A is -87.91 dBc/Hz, while that of case B is -80.13 dBc/Hz. As the spectral mask of MICS band only requires the attenuation of 20 dB at the edge of the 300 kHz-channel, the phase noise requirement of the transmitter is relaxed. Therefore, the phase noise degradation is tolerable at VDD $= 0.6$ V, while $\sim 3\times$ power saving is achieved.

The locking range of the transmitter can be estimated from the transition point in the phase noise plot when it is locked (Fig. 2), which is approximately 1 MHz. The locking of the SHILRO is guaranteed by tuning the free running frequency of the ring oscillator off-chip to make it close to that of the injected signal.

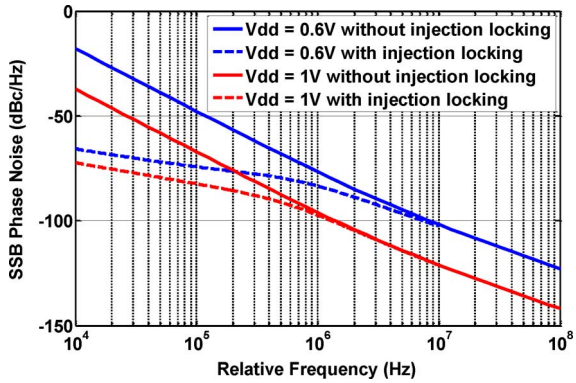


Fig. 2. Phase noise with and without injection locking at VDD $= 0.6$ V, 1 V.

In real application, frequency locked loop can be performed to calibrate the oscillator free running frequency.

C. Spur Suppression

There are several sources within the oscillator that may introduce large spurious tones in the frequency multiplied output, affecting the spectral purity. These periodic perturbations of the oscillator phase at the injected signal frequency are typically deterministic, arising from rich harmonic coupling of the injected signal, multiphase mismatches at the summing node of the SHILRO output, and any process variations within the edge combiner.

With sub-harmonic injection locking, the injected signal is typically a square-wave pulse waveform consisting of large harmonic content. However, only the N-th harmonic locks the oscillator while the others appear at the output as spurs with limited suppression. The relative spur level is as follows [23]:

$$\frac{|A_{\rm spur}|}{|A_{{\rm out},\omega_{\rm inj}}|} = \frac{\omega_L}{\omega_m} \tag{2}$$

where $\omega_{\rm L}$ is the locking range and $\omega_{\rm m}$ is the frequency difference between the spurious tone and the desired one. Hence, decreasing the locking range can increase the spur suppression, at the cost of increased locking time and the increased probability of losing lock. There is also a tradeoff with phase noise performance, since the locking-range $\omega_{\rm L}$ also determines the loop bandwidth for the amount of phase noise rejection.

Multiphase asymmetry can contribute to significant increases in spur-to-carrier ratio. These unequal phase spaces can arise due to asymmetric single-phase injection into the ring [12], [16], device variations such as $V_{\rm TH}$ mismatches under low supply voltage, and capacitive layout mismatches observed in the wiring breakout from the ring oscillator. For example, transistor mismatches within the edge combiner can result in large spurs in the combined output waveform (Fig. 3). While this reference spur is exacerbated when operating at low-VDD, these phase offsets are low-frequency in nature and can be minimized at chip startup. In this work, individual phase calibration is performed open-loop without on-chip phase detection. On-chip, closed-loop multiphase timing detection/calibration

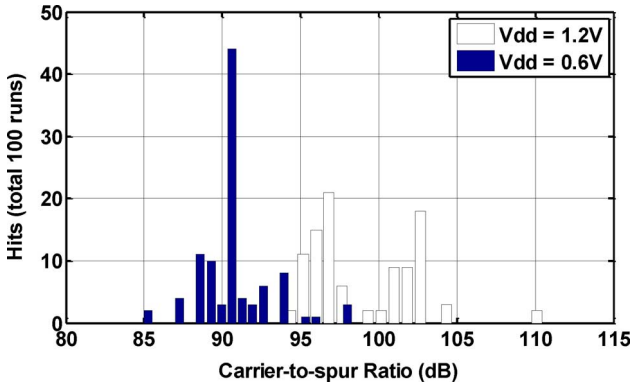


Fig. 3. Carrier-to-spur ratio caused by mismatches in the edge combiner.

has been previously shown in [24], demonstrating sub-2 ps phase resolution.

IV. Noise-Rejecting Super-Regenerative Receiver

A. Theory of Super-Regeneration and Q-Enhancement

Super-regeneration exploits the non-linear gain observed during startup of an LC oscillator. An equivalent circuit model of an LC oscillator with an injected signal is shown in Fig. 4. $A\sin(\omega t)$ represents the received signal, $R_{\rm p}$ is the parasitic losses within the LC tank, $-G_{\rm m}$ is the negative conductance produced by a cross-coupled differential pair, and $V_{\rm o}$ is the differential voltage across the tank. The second order differential equation written with KCL [25], [26] is given by

$$A\sin(\omega t) = C\frac{dV_o}{dt} + GV_o + \frac{1}{L}\int V\,dt \tag{3}$$

where $G = R_{\rm p}^{-1} - G_{\rm m}$ is the effective conductance. Solving the equation to get $V_{\rm o}$, the result is

$$V_o = e^{-\alpha t}(k_1\cos(\omega_d t) + k_2\sin(\omega_d t)) + \frac{A\sin(\omega t+\phi)}{\sqrt{G^2+(\omega C - 1/\omega L)^2}} \tag{4}$$

where

$$\alpha = \frac{G}{2C}. \tag{5}$$

$$\omega_d = \sqrt{\omega_o^2 - \alpha^2}. \tag{6}$$

$$\omega_o = \frac{1}{\sqrt{LC}}. \tag{7}$$

$$k_1 = V_o(0^+). \tag{8}$$

$$k_2 = \frac{\frac{dV_o(0^+)}{dt} + \alpha k_1}{\omega_d}. \tag{9}$$

The first term in (4) is the transient oscillation at frequency $\omega_{\rm d}$ with the damping factor α, describing the circuit's natural response while the second term represents the response to the injected signal. When G is positive, the active device cannot produce enough energy to compensate for the loss inside the LC tank and the natural response dies out, leaving only the second term. Super-regeneration occurs when G is negative. In this situation, the oscillation builds up from the initial voltage on the tank and increases in magnitude regardless of the applied injected signal, thereby achieving exponential time-dependent gain.

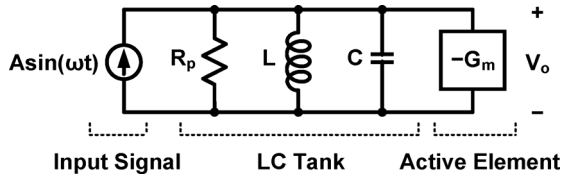


Fig. 4. Equivalent circuit model of the super-regenerative oscillator.

To improve frequency selectivity of the SRR, Q-enhancement technique is employed. The second term in (4) describes a band-pass filtering characteristic where the oscillation amplitude builds up. The effective oscillation Q is calculated as

$$Q_{\rm eff} = \frac{1}{G}\frac{1}{\sqrt{L/C}}. \tag{10}$$

Hence, a very high-Q filter is achievable when G is positive and close to 0. Even with a relatively low tank Q, usually from 10–100, the effective oscillator Q can be more than 1000. Because G can be tuned by changing the tank current, the conductance can be made very close to 0, with this corresponding tank current called the critical current $I_{\rm crit}$.

To detect any injected RF signal, the digitally-controlled oscillator (DCO) is first set in the Q-enhancement mode (without amplification but with good selectivity) to select the band of interest. In this mode, it works as a high-Q band-pass filter. Then, the effective conductance of the DCO is switched from positive to negative by increasing the tank current, thereby achieving super-regeneration that non-linearly amplifies the selected signal. In order to achieve large gain ($e^{-\alpha t}$), either the time to build up oscillation or the absolute value of the negative conductance should be increased. The SRR only responds to the injected signal when the oscillator's effective conductance turns negative, such that a periodical quench signal is required to control this conductance.

There exists a trade-off between selectivity and start-up time. The time required for oscillation build-up not only depends on the initial voltage on the tank, but also on the value of α. The larger the value of $|G|$, i.e., the larger the value of $|\alpha|$, the faster the oscillation starts up (gain is represented by $e^{-\alpha t}$). However, a smaller value of $|G|$ is also preferred since good selectivity results when $|G|$ is close to 0. Hence, by increasing the current slowly when G crosses the 0 threshold slowly, the selectivity can be improved, considering that the injected signal is a sine wave and the zero crossing of G may not align with the peak of the injected signal. Based on this analysis, a slow start-up with high selectivity is desired, reducing the data rate. However, the current can be raised with a steep slope to the critical current and then with a reduced slope around the critical current. In addition to optimizing this slope of this rising current, the use of a proceeding high-sensitivity comparator relaxes the required

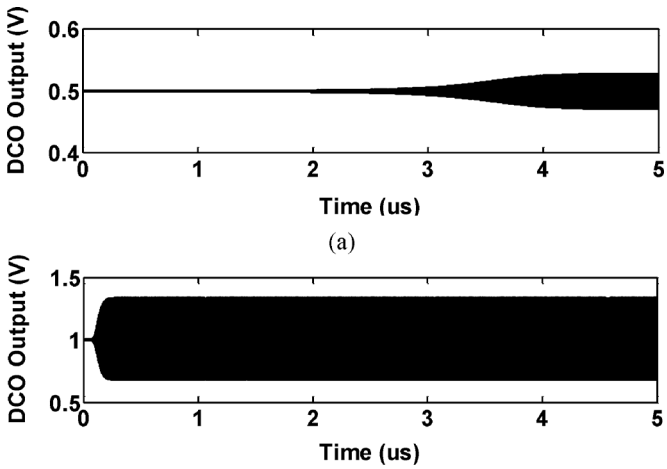


Fig. 5. Simulated output waveforms of DCO at (a) VDD $=$ 0.5 V and (b) VDD $=$ 1 V, with the same received input signal.

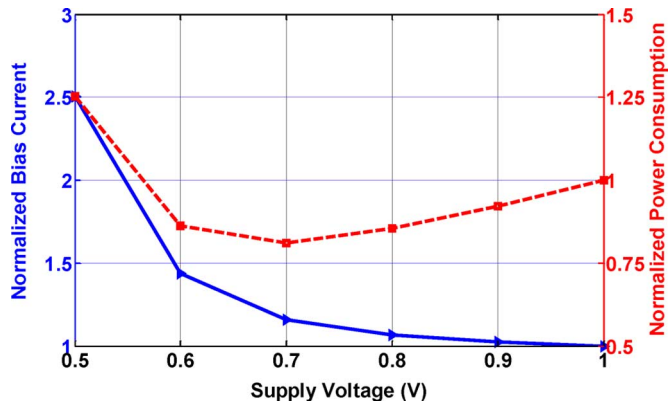


Fig. 6. Normalized bias current and power consumption of the DCO at different supply voltages to achieve oscillation at the same time (1 μs).

amplitude of the oscillator. The detailed quench mechanism and fast start-up circuit implementations are presented in Section V.

B. Super-Regenerative Operation at Low-VDD

As mentioned previously, low-voltage operation can significantly improve the power efficiency. However, the reduction in supply voltage reaches a finite limit before any further supply reduction degrades the performance nonlinearly as VDD nears the threshold voltage.

The frequency of the LC oscillator is mainly determined by the values of the inductance and capacitance. To improve the robustness of the system, a constant-$G_{\rm m}$ biasing circuit is implemented and helps to overcome any process mismatches and threshold voltage variations that arise as VDD is lowered. Eventually, the problem of reduced headroom under low-voltage operation arises. The lower-VDD reduces the $G_{\rm m}$ of the cross-coupled pair, resulting in the degradation of the start-up speed and failure to achieve oscillation, if $G_{\rm m}$ is decreased too much. Low supply voltage also lowers the oscillator output swing, affecting the minimum required sensitivity for the proceeding envelope detector and comparator. As seen in Fig. 5, the startup speed and output swing of the DCO is significantly impacted when VDD $=$ 0.5 V versus at VDD $=$ 1.0 V, negatively affecting the maximum data rate. Hence, if a required date rate is desired, the bias current at lower supply voltage should be increased to force the DCO to oscillate earlier. As shown in Fig. 6, the bias current of the DCO at VDD $=$ 0.5 V need to achieve oscillation within 1 μs is $\sim$2.5$\times$ that required at VDD $=$ 1.0 V. Hence, for optimal power consumption, a balance is made between lowering VDD and increasing DCO current, resulting in an optimal biasing when VDD $=$ 0.75 V.

C. Replica SRR for Increased Noise Immunity

Robustness and immunity to on-chip noise coupling is an important consideration for MICS applications. For a conventional OOK super-regenerative receiver [25], the DC reference into the differential comparator is fixed such that it is very sensitive to on-chip noise coupling. Furthermore, when the DCO is biased in the extremely high-gain mode, any perturbations in the LC tank can cause the oscillator to begin oscillating, even if no received signal is applied. This is especially problematic for OOK modulation, as the duration of time when no signal is transmitted can actually be extremely noisy.

The proposed receiver is designed to be immune to noise coupling by introducing a replica LNA-DCO-ENV, as shown in Fig. 1. The replica SRR generates a reference envelope for the comparator so that any unwanted noise sources (i.e., on-chip supply noise, large transient noises during OFF keying) appear common-mode to both super-regenerative receivers. As a result of this receiver architecture, the decision comparator differentially receives two envelopes—one with the real input data and the other with the replica bias chain. Hence, any supply noise or feed-through coupling can be rejected. Besides, the replica LNA is disabled during normal operation, the power overhead of the replica chain is quite small.

V. Circuit Implementation

A. Sub-Harmonic Injection-Locked Ring Oscillator

The proposed injection-locked oscillator consists of an AC-coupled injection stage (Fig. 7) and a five-stage, single-ended, current-starved, ring oscillator, where each stage shares a 32 b thermometer-encoded current source. Due to VDD operation in the near-threshold domain, the drain-source voltages of the tail transistors that comprise the current source are extremely small ($\sim$20 mV). Hence, these tail current source transistors operate in the triode region as opposed to the desired saturation region. Therefore, these "current-source" transistors are treated as resistors rather than current mirrors, where the RC time constant of the ring-based oscillator is dominated by the resistance of these tail transistors, not the delay cells. In order to linearize the tuning range of the oscillation frequency, the total shunt resistance of the parallel-activated tail transistors should decrease linearly as the thermometer code bits are

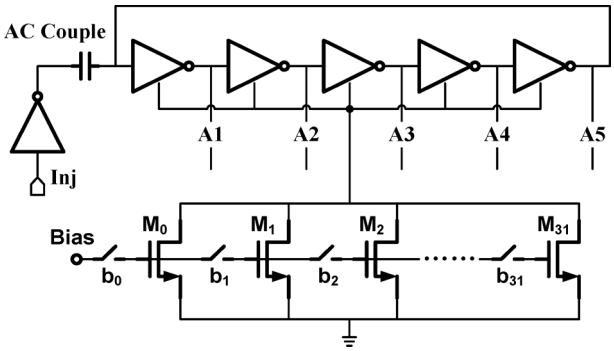


Fig. 7. Schematic of the sub-harmonic injection-locked oscillator.

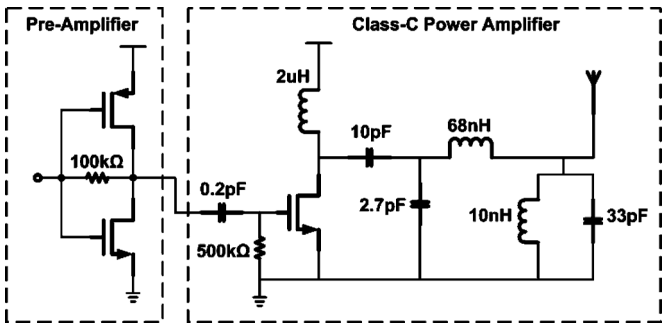


Fig. 8. Schematic of the pre-amplifier and the power amplifier.

increased. Hence, the sizes of these current-source transistors are pre-distorted to a series of specific values as follows:

$$\begin{cases} \left(\dfrac{W}{L}\right)_0 = \dfrac{1}{32} \\ \left(\dfrac{W}{L}\right)_n = \dfrac{1}{(32-n)(33-n)}, \quad n = 1, 2, \ldots, 31 \end{cases} . \tag{11}$$

This gives the total shunt resistance of the activated tail transistors as

$$R_{\text{total}} = 32 - n \tag{12}$$

if all transistors M_0 through M_n are activated. Hence, a linear frequency tuning range can be achieved using these resistor-like transistors, when operating under low-VDD conditions.

B. Pre-Amplifier and Class-C Power Amplifier

As shown in Fig. 8, due to its energy-efficient structure, an inverter-based pre-amplifier is chosen to boost the amplitude of 400 MHz edge combiner output. The use of the class-C power amplifier requires a large input voltage swing at the gate, as it is biased in the cut-off region. The output matching network and the antenna are placed off-die to reduce the die area since the component values are large at 400 MHz.

C. LNA, Super-Regenerative Oscillator, and Envelope Detector

The schematics of the LNA, super-regenerative oscillator and envelope detector are shown in Fig. 9. As opposed to signal injection directly into the oscillator tank, the LNA stage improves

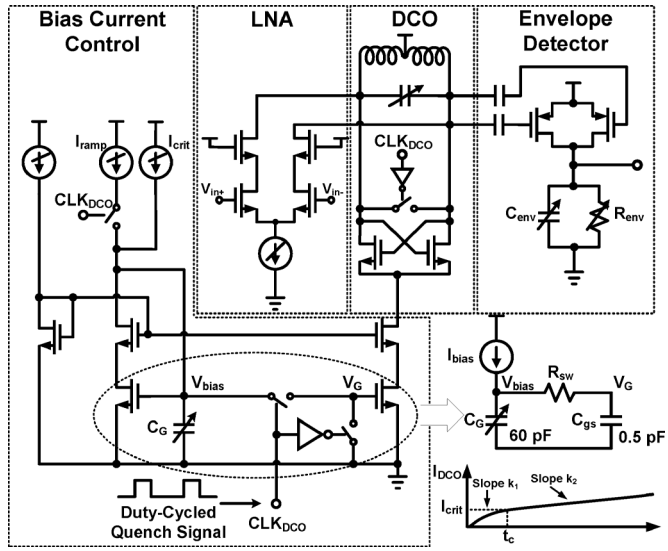


Fig. 9. Schematic of the LNA, the super-regenerative oscillator, and the envelope detector.

tank isolation and prevents the DCO signal from kicking back into the antenna.

A differential NMOS topology with only two stacked transistors is adopted for the VCO, as this topology provides higher output swing under a low-supply voltage. The band-pass frequency of the super-regenerative oscillator can be tuned using digitally-controlled capacitor banks that cover the entire MICS frequency band. The DCO can be fine-grained duty-cycled by controlling the quench signal $\mathrm{CLK_{DCO}}$, resulting in significant power saving when the transceiver is idle. An external high-Q air-coil of 18.5 nH is used as the inductor to reduce the required bias current.

The outputs of the DCO are connected to an envelope detector. A low-pass filter (LPF) load in the envelope detector reduces the high frequency components at the output while a tunable resistor and capacitor enable bandwidth control.

D. DCO Bias Current Control and Fast Start-Up Technique

To receive OOK data, the DCO is quenched periodically at the same rate as the incoming data. Since the negative conductance $-G_\mathrm{m}$ is controlled by the bias current of the oscillator, the quench mechanism which determines the bias current can be optimized to improve the SRR performance.

The oscillator can be heavy duty-cycled, and immediately quenched after data is received, resulting in improved power savings. The bias current of the oscillator is composed of a critical current I_{crit} and a ramp-up current I_{ramp} as shown in Fig. 9, where I_{crit} is the minimum current resulting in oscillation and I_{ramp} is enabled periodically as the quench signal. The bias current reaches I_{crit} quickly, and then slowly ramps up after reaching the critical current, improving the selectivity and sensitivity. In [25], an on-chip, closed-loop calibration to determine the value of I_{crit} is shown. In this work, I_{crit} is calibrated open-loop.

A fast start-up technique is introduced by adding a large charged capacitor C_G to at the gate of the bias transistor. This

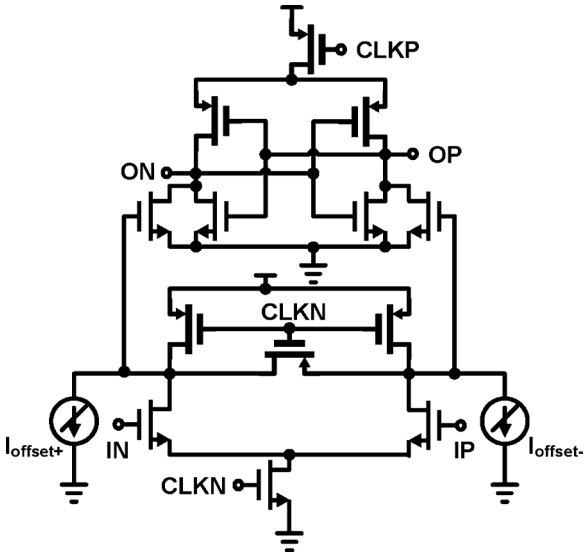


Fig. 10. Schematic of the offset calibrated comparator.

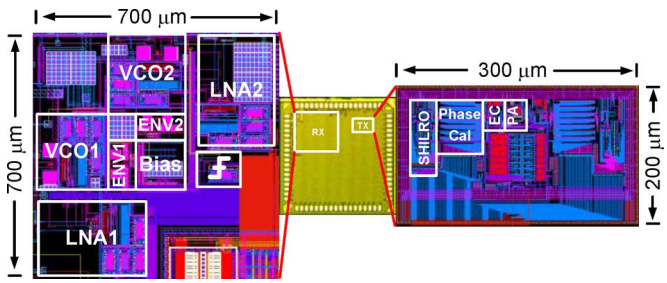


Fig. 11. Photomicrograph of the transceiver.

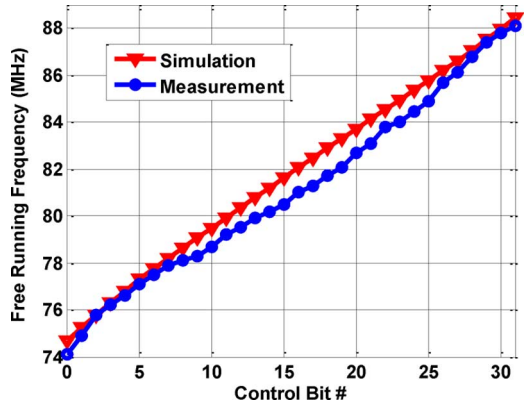


Fig. 12. Measured SHILRO tuning range.

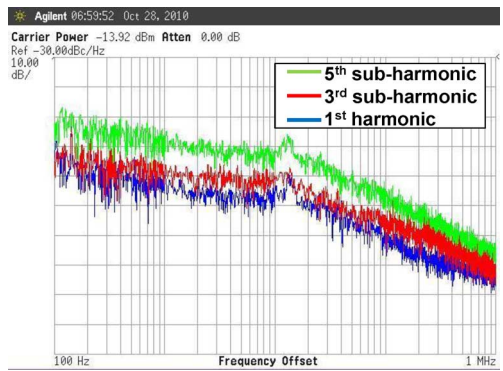


Fig. 13. Measured phase noise of the injection-locked ring oscillator for different injection frequencies.

capacitor reduces the settling time t_c required to reach the critical current, thereby maximizing the data rate and reducing the power consumption. The values of C_G and I_{ramp} are digitally programmable in order to adjust the ramp-up time.

E. Comparator With Offset Calibration

To accurately measure the oscillation envelope, a sense-amplifier-based low-power comparator with offset calibration is used, as shown in Fig. 10 [27]. There is no static current, and at low data rate the dynamic power consumption is less than 1 μW. Simulations and measurements confirm that after offset calibration, a minimum sensitivity of several millivolts is achieved.

VI. Measurement Results

The transceiver was fabricated in 90-nm CMOS technology. The transmitter and the receiver consume 0.06 mm^2 and 0.49 mm^2 of active area, respectively, as shown in Fig. 11. The radio shares the same die with other SoC blocks such as the CPU, ADC and front-end bio-sensor amplifier. The power consumption of the transmitter and the receiver are 160 μW (VDD $=$ 0.6 V) and 180 μW (VDD $=$ 0.8 V), respectively, for a data rate of 1 Mbps.

A. Transmitter

Fig. 12 shows the simulated and measured SHILRO frequency tuning range. With the pre-distorted tail current-source transistors, the free running frequency of the SHILRO can be adjusted at a nearly constant 450 kHz step across the entire tuning range of 74–88 MHz ($\sim$17%). The measured phase noise level (Fig. 13) of the SHILRO with 3rd (26.7 MHz) and 5th (16 MHz) sub-harmonics are 10 dB and 15 dB higher than that of the 1st (80 MHz) harmonic, respectively, corresponding to the predicted $20\log_{10} N$ vertical separation. The output spectral mask of transmitter is shown in Fig. 14, which meets the MICS spectral mask requirement. The carrier-to-spur ratio of the local oscillator improves by 9 dB when per-phase timing calibration is performed (Fig. 15) to minimize multiphase timing offsets. The TX output power is -17 dBm at a data rate of 1 Mbps.

B. Receiver

Fig. 16 shows the tuning of the DCO with a 5-bit digitally controlled capacitor bank. The DCO tunes from 392.16–416.94 MHz with an average tuning step of 800 kHz, covering the MICS frequency band of 402–405 MHz. The measured time domain signals of the receiver with a 1 Mbps data-rate are shown in Fig. 17. Shown are the received OOK signal, the quench signal $\mathrm{CLK_{DCO}}$, the differential output of the envelope detectors, and the demodulated data. When a "1" appears, the DCO will start to oscillate earlier with the quench signal. The oscillation envelope is detected and both the output from the main signal SRR and the replica chain SRR are sent to the differential inputs of the comparator to

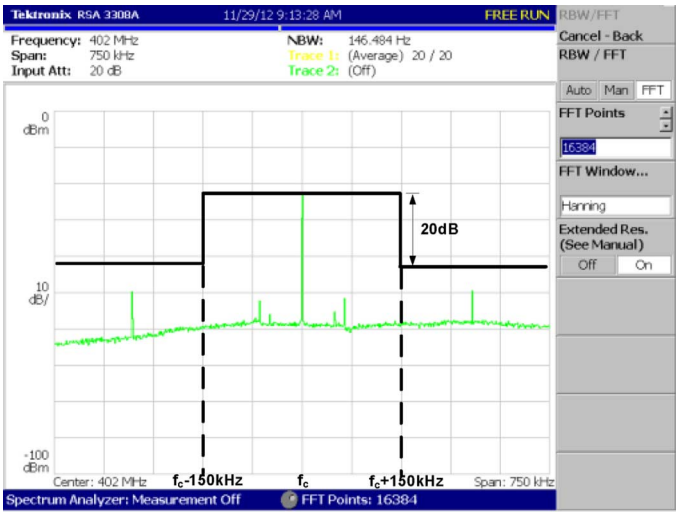


Fig. 14. Measured spectral mask of transmitter with a data rate of 1 Mbps.

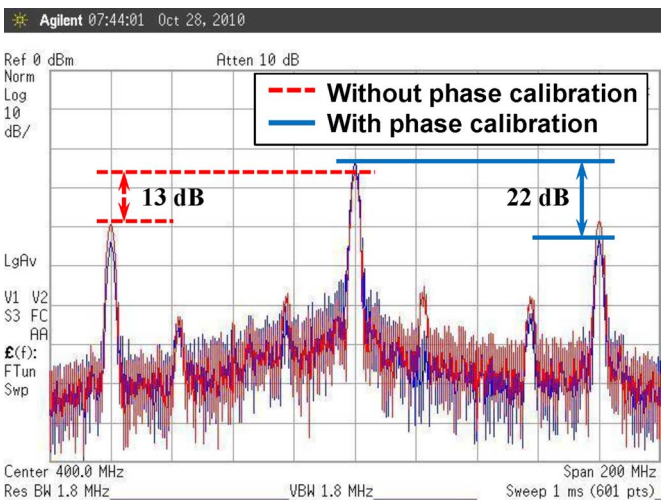


Fig. 15. Measured carrier-to-spur ratio before and after individual phase calibration.

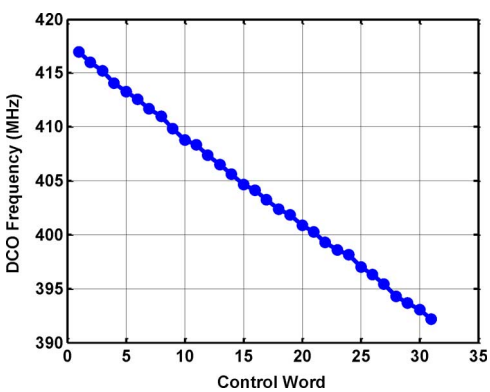


Fig. 16. Measured DCO frequency tuning range.

demodulate the OOK data. The mismatch between the two chains can be calibrated before detecting the RF signal. Fig. 18 shows the measurements results before and after the proposed noise cancellation technique is applied. When the replica

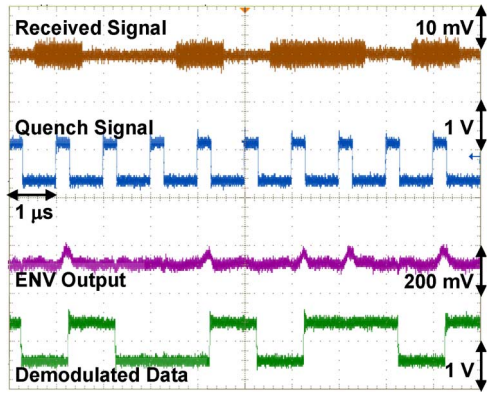
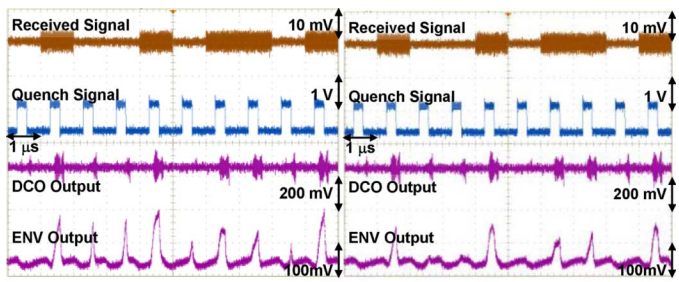


Fig. 17. Measured receiver time domain outputs for a data rate of 1 Mbps.



(a) (b)

Fig. 18. Measured receiver time domain outputs (a) without noise cancellation and (b) with noise cancellation.

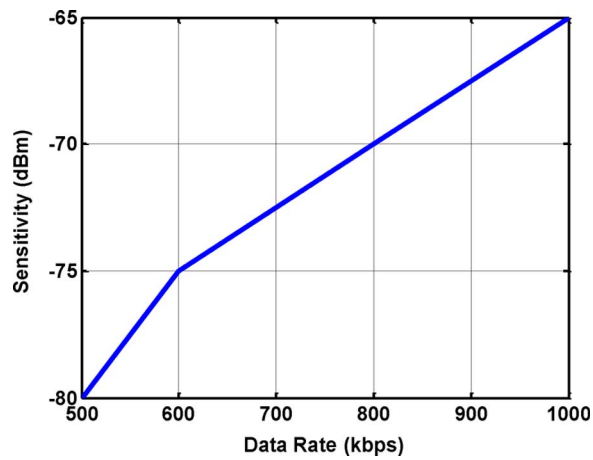


Fig. 19. Measured sensitivity versus data-rate.

LNA-DCO-ENV chain is disabled, the DCO erroneously oscillates in the presence of on-chip noise even without any applied input RF signal, causing errors in the demodulated output. By enabling the replica LNA-DCO-ENV chain, the noise appears common-mode to both SRRs, thereby mitigating any differential envelope seen by the comparator, as shown in Fig. 18(b). The tradeoff between sensitivity and data rate is shown in Fig. 19. At low data rate the SRR can achieve better sensitivity, since it has more time to build-up oscillation. The receiver achieves high selectivity, as shown in Fig. 20, with a signal rejection better than -15 dB at a 3 MHz frequency offset. Table I summarizes the entire transceiver performance

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

TX Parameter	**[10]**	**[11]**	**[12]**	**[29]**	**[30]**	**THIS WORK**
Technology	90 nm	180 nm	130 nm	180 nm	180 nm	90 nm
Modulation	MSK	FSK	FSK	BFSK	FSK	OOK
Data Rate	120 kbps	250 kbps	200 kbps	800 kbps	50 kbps	1 Mbps
Supply	0.7 V	0.7 V	1 V	2.1-3.5 V	1.8 V	0.6-1.0 V
Power	350 μW	400 μW	90 μW	>10 mW	4.9 mW	160 μW (VDD = 0.6V)
Energy per Bit	2.9 nJ/b	1.6 nJ/b	0.45 nJ/b	>12.5 nJ/b	98 nJ/b	0.16 nJ/b
Output power	NA	-16 dBm	-17 dBm	-17~-4 dBm	-20~0 dBm	-17 dBm
RX Parameter	**[10]**	**[11]**	**[28]**	**[29]**	**[30]**	**THIS WORK**
Technology	90 nm	180 nm	130 nm	180 nm	180 nm	90 nm
Modulation	OOK	FSK	FSK	FSK	FSK	OOK
Architecture	Super-reg.	Low-IF	Low-IF	Low-IF	Low-IF	Super-reg.
Sensitivity (BER=10^{-3})	-93 dBm @ 120 kbps -99 dBm @ 40 kbps	-98 dBm @ 250 kbps	-90 dBm @ Main mode -70 dBm @ LP mode	<20 μV_{rms} @ 200 kbps	35 μV_{rms} @ 200 kbps	-65 dBm @ 1 Mbps -80 dBm @ 500 kbps (VDD = 0.8 V)
Supply	0.7 V	0.7 V	1 V	2.1-3.5 V	1.8 V	0.7-1 V
Power	400 μW	490 μW	120 μW	>10 mW	10.8 mW	180 μW (VDD = 0.8V)
Energy per Bit	10 nJ/b @ 120 kbps 3.3 nJ/b @ 40 kbps	1.96 nJ/b @ 250 kbps	0.6 nJ/b @ Main mode 0.22 nJ/b @ LP mode	>12.5 nJ/b @ 800 kbps	54 nJ/b @ 200 kbps	0.18 nJ/b @ 1 Mbps 0.256 nJ/b @ 500 kbps (VDD = 0.8 V)

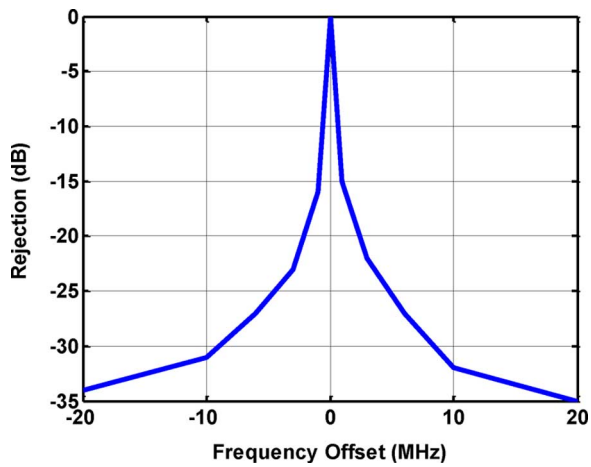


Fig. 20. Measured out-of-band signal rejection at a data rate of 1 Mbps.

and compares this design with other recently published MICS transceivers.

VII. CONCLUSION

In this paper, a near-threshold transceiver for the MICS band was presented. Because it is optimized to operate with a low supply voltage, energy efficiency is greatly improved. The transmitter utilizes sub-harmonic injection-locked ring oscillator and edge combining to achieve low-power frequency multiplication. A pre-distorting resistor linearization technique is used to achieve linear tuning range of the TX local oscillator while operating under low-VDD. The super-regenerative receiver exhibits good sensitivity and selectivity performance at low-VDD. To address the problem of sensitivity to background switching noise, a replica super-regenerative oscillator is proposed. The measured transmitter and receiver achieve an energy-per-bit of 0.16 nJ/b and 0.18 nJ/b, respectively.

ACKNOWLEDGMENT

The authors would like to thank Prof. G. Cauwenberghs and Prof. G. Temes for technical discussions and insights.

REFERENCES

[1] E. Jovanov, "Wireless technology and system integration in body area networks for m-health applications," in *Proc. 27th Annu. Int. Conf. IEEE Engineering in Medicine and Biology Soc.*, Sep. 2005, pp. 7158–7160.

[2] L. Huang, M. Ashouei, F. Yazicioglu, J. Penders, R. Vullers, G. Dolmans, P. Merken, J. Huisken, H. de Groot, C. Van Hoof, and B. Gyselinckx, "Ultra-low power sensor design for wireless body area networks: Challenges, potential solutions, and applications," *Int. J. Digit. Content Technol. Appl.*, vol. 3, no. 3, pp. 136–148, Sep. 2009.

[3] A. C. W. Wong, D. McDonagh, O. Omeni, C. Nunn, M. H. Silveira, and A. J. Burdett, "Sensium: An ultra-low-power wireless body sensor network platform: Design & application challenges," in *Proc. 31st Ann. Int. Conf. IEEE Engineering in Medicine and Biology Soc.*, Sep. 2009, pp. 6576–6579.

[4] A. C.-W. Wong, D. McDonagh, G. Kathiresan, O. C. Omeni, O. El-Jamaly, T. C.-K. Chan, P. Paddan, and A. J. Burdett, "A 1 V, micropower system-on-chip for vital-sign monitoring in wireless body sensor networks," in *Proc. IEEE Int. Solid-State Circuits Conf., Dig. Tech. Papers*, Feb. 2008, pp. 138–139.

[5] O. Omeni, A. C. W. Wong, A. J. Burdett, and C. Toumazou, "Energy efficient medium access protocol for wireless medical body area sensor networks," *IEEE Trans. Biomed. Circuits Syst.*, vol. 2, no. 4, pp. 251–259, Dec. 2008.

[6] C. Hu, S. Redfield, H. Liu, R. Khanna, J. Nejedlo, and P. Chiang, "Transmitter equalization for multipath interference cancellation in impulse radio ultra-wideband (IR-UWB) transceivers," in *Proc. VLSI Design, Automation and Test Symp.*, Apr. 2009, pp. 307–310.

[7] P. Chiang, S. Woracheewan, C. Hu, L. Guo, R. Khanna, J. Nejedlo, and H. Liu, "Short-range, wireless interconnect within a computing chassis: Design challenges," *IEEE Des. Test Comput.*, vol. 27, no. 4, pp. 32–43, Mar. 2010.

[8] J. L. Bohorquez, A. P. Chandrakasan, and J. L. Dawson, "Frequency domain analysis of super-regenerative amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 12, pp. 2882–2894, Dec. 2009.

[9] MICS Band Plan Federal Commun. Comm., Part 95, FCC Rules and Regulations, Jan. 2003.

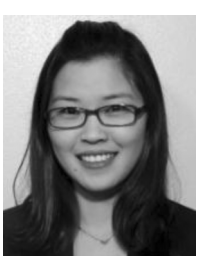
[10] J. L. Bohorquez, A. P. Chandrakasan, and J. L. Dawson, "A 350 μW CMOS MSK transmitter and 400 μW OOK super-regenerative receiver for medical implant communications," *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1248–1259, Apr. 2009.

[11] J. Bae, N. Cho, and H. J. Yoo, "A 490 μW fully MICS compatible FSK transceiver for implantable devices," in *Proc. Symp. VLSI Circuits, Dig. Tech. Papers*, Jun. 2009, pp. 36–37.

[12] J. Pandey and B. P. Otis, "A sub-100 μW MICS/ISM band transmitter based on injection-locking and frequency multiplication," *IEEE J. Solid-State Circuits*, vol. 46, no. 5, pp. 1049–1058, May 2011.

[13] A. Chandrakasan, N. Verma, J. Kwong, D. Daly, N. Ickes, D. Finchelstein, and B. Calhoun, "Micropower wireless sensors," in *Proc. Nano Science and Technology Institute Nanotech Conf.*, May 2006, vol. 3, pp. 459–462.

[14] S. C. Jocke, J. F. Bolus, S. N. Wooters, A. D. Jurik, A. C. Weaver, T. N. Blalock, and B. H. Calhoun, "A 2.6-μW sub-threshold mixed-signal ECG SOC," in *Proc. Symp. VLSI Circuits, Dig. Tech. Papers*, Jun. 2009, pp. 60–61.
[15] L. Xia, K. Shao, H. Chen, Y. Huang, Z. Hong, and P. Y. Chiang, "0.15-nJ/b 3–5-GHz IR-UWB system with spectrum tunable transmitter and merged-correlator noncoherent receiver," *IEEE Trans. Microw. Theory Tech.*, vol. 59, no. 4, pp. 1147–1156, Apr. 2011.
[16] K. Hu, T. Jiang, J. Wang, F. O'Mahony, and P. Chiang, "A 0.6 mW/Gb/s, 6.4–7.2 Gb/s serial link receiver using local, injection-locked ring oscillators in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 899–908, Apr. 2010.
[17] D. Werber, A. Schwentner, and E. M. Biebl, "Investigation of RF transmission properties of human tissues," *Adv. Radio Sci.*, vol. 4, pp. 357–360, 2006.
[18] C. Hu, P. Y. Chiang, K. Hu, H. Liu, R. Khanna, and J. Nejedlo, "A 90 nm-CMOS, 500 Mbps, fully-integrated IR-UWB transceiver using pulse injection-locking for receiver phase synchronization," in *Proc. IEEE Radio Frequency Integrated Circuits Symp. Dig.*, 2010, pp. 201–204.
[19] J. Lee and H. Wang, "Study of subharmonically injection-locked PLLs," *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1539–1553, May 2009.
[20] D. B. Leeson, "Simple model of a feedback oscillator noise spectrum," *Proc. IEEE*, vol. 54, no. 2, pp. 329–330, Feb. 1966.
[21] A. P. Chandrakasan, D. C. Daly, D. F. Finchelstein, J. Kwong, Y. K. Ramadass, M. E. Sinangil, V. Sze, and N. Verma, "Technologies for ultradynamic voltage scaling," *Proc. IEEE*, vol. 98, no. 2, pp. 191–214, Feb. 2010.
[22] A. Hajimiri, S. Limotyrakis, and T. H. Lee, "Jitter and phase noise in ring oscillators," *IEEE J. Solid-State Circuits*, vol. 34, no. 6, pp. 790–804, Jun. 1999.
[23] S. Dal Toso, A. Bevilacqua, M. Tiebout, S. Marsili, C. Sandner, A. Gerosa, and A. Neviani, "UWB fast-hopping frequency generation based on sub-harmonic injection locking," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2844–2852, Dec. 2008.
[24] L. Xia, J. Wang, W. Beattie, J. Postman, and P. Chiang, "Sub-2 ps, static phase error calibration technique incorporating measurement uncertainty cancellation for multi-gigahertz time-interleaved T/H circuits," *IEEE Trans. Circuits Syst. I. Reg. Papers*, vol. 59, no. 2, pp. 276–284, Aug. 2011.
[25] J. Y. Chen, M. P. Flynn, and J. P. Hayes, "A fully integrated auto-calibrated super-regenerative receiver in 0.13-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 42, no. 9, pp. 1976–1985, Sep. 2007.
[26] J. W. Nilsson and S. A. Riedel, *Electric Circuits*. Reading, MA, USA: Addison-Wesley, 1996.
[27] D. Schinkel, E. Mensink, E. Klumperink, E. van Tuijl, and B. Nauta, "A double-tail latch-type voltage sense amplifier with 18 ps setup+hold time," in *Proc. IEEE Int. Solid-State Circuits Conf., Dig. Tech. Papers*, Feb. 2007, pp. 314–315.
[28] J. Pandey, J. Shi, and B. P. Otis, "A 120 μW MICS/ISM-band FSK receiver with a 44 μW low-power mode based on injection-locking and 9$\times$ frequency multiplication," in *Proc. IEEE Int. Solid-State Circuits Conf., Dig. Tech. Papers*, Feb. 2011, pp. 460–461.
[29] P. Bradley, "An ultra low power, high performance medical implant communication system (MICS) transceiver for implantable devices," in *Proc. IEEE Biomedical Circuits and Systems Conf.*, Dec. 2006, pp. 158–162.
[30] N. Cho, J. Bae, and H.-J. Yoo, "A 10.8 mW, body channel communication/MICS dual-band transceiver for a unified body sensor network controller," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3459–3468, Dec. 2009.

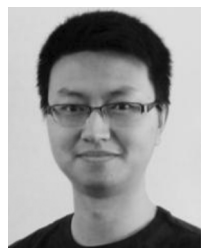


Chao Ma (S'12–M'13) received the B.S. degree in electrical engineering from Southeast University, Nanjing, China, and the M.S. degree in electrical and computer engineering from Oregon State University, Corvallis, OR, USA, in 2009 and 2012, respectively.

Since 2012, she has been with Marvell Technology Ltd., Shanghai, China, working on low-power Zigbee products.

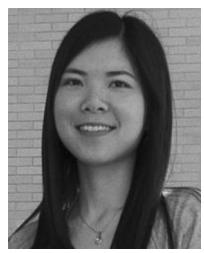
Changhui Hu (S'08–M'11) received the B.S. degree in electrical engineering from the Huazhong University of Science and Technology, Wuhan, China, the M.Eng. degree in electrical engineering from Nanyang Technological University, Singapore, and the Ph.D. degree in electrical engineering from Oregon State University, Corvallis, OR, USA, in 2001, 2006, and 2011, respectively.

From August 2001 to November 2002, he was a Research Assistant at the Centre for Wireless Communications (later known as the Institute for Communications Research and now Institute for Infocomm Research, ASTAR), Singapore. From December 2002 to April 2005, he was with Advanced RFIC Singapore as an RF/Analog IC Designer. From May 2005 to July 2006, he was with OKI Techno Center Singapore (now known as Wipro Techno Center), where he worked on WLAN and UWB projects. From August 2006 to September 2007, he worked as a Corporate Application Engineer at Mentor Graphics Asia, supporting Calibre products. Since April 2011, he has worked on Wi-Fi products at Marvell Semiconductor, Santa Clara, CA, USA, as a Senior RF/Analog IC Design Engineer.



Jiao Cheng (S'10) received the B.E. degree in microelectronics from Tsinghua University, Beijing, China, in 2009.

Currently, he is working toward the Ph.D. degree in electrical engineering at Oregon State University, Corvallis, OR, USA. In 2012, he was a summer intern at Broadcom Corporation, Irvine, CA, USA. His current research interests include low-power, short-range wireless transceivers and medical sensor-on-a-chip design.



Lingli Xia received the B.S. degree in electronics science and technology from the Huazhong University of Science and Technology, Wuhan, China, and the Ph.D. degree in microelectronics and solid state electronics from Fudan University, Shanghai, China, in 2005 and 2010, respectively.

Currently, she is doing postdoctoral work in electrical engineering at Oregon State University, Corvallis, OR, USA. Her doctoral thesis concerns ultra-wideband RF transceiver design. Her research interests include RF front-end circuit and digital baseband circuit for wireless communication systems.

Patrick Yin Chiang (S'99–M'07) received the B.S. degree in electrical engineering and computer sciences from the University of California, Berkeley, Berkeley, CA, USA, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, USA, in 1998, 2001, and 2007, respectively.

Currently, he is an Associate Professor (on sabbatical) at Oregon State University, Corvalis, OR, USA. He is also a 1000-Talents Young Professor at the ASIC and System State Key Laboratory at Fudan University, Shanghai, China. In 1998, he was a Design Engineer at Datapath Systems (now LSI), where he designed a low-power, standard cell library for xDSL. In 2003, he was a Research Intern at Velio Communications (now Rambus), investigating 10 GHz clock synthesis techniques. In 2004, he worked as a Consultant at Telegent Systems (now Spreadtrum), where he analyzed low-phase VCOs for TV tuners. In 2006, he was a Visiting NSF Research Fellow at Tsinghua University, Beijing, China, investigating super-regenerative RF transceivers. His interests are in energy-efficient circuits and systems, such as low-power wireline and photonic interfaces, energy-constrained medical sensors, and reliable near-threshold computing.

Dr. Chiang was the recipient of a 2010 Department of Energy Early Career Award and a 2012 NSF-Career Award. He is an associate editor of IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS, and on the technical program committee for the IEEE Custom Integrated Circuits Conference.