2/19/15:

Energy Reduction in Weakly Hard Real Time Systems
A Schedulability Analysis for Weakly Hard Real-Time Tasks in Partitioning Scheduling on Multiprocessor Systems

1. Describe two main defining characteristics of a weakly hard real time embedded system that is unique to these types of systems
2. What is the Inverse Rate Monotonic Algorithm?
3. How are the mandatory tasks and optional tasks scheduled in offline scheduling?

A Hardware-Scheduler for Fault Detection in RTOSBased Embedded Systems
ARINC 653 Interface in RTEMS

4. What is Spatial Segregation?
5. Why is Spatial Segregation and Temporal partitioning so important to fault tolerant real time applications?
6. What is the issue with putting many different fault tolerant mechanisms in an RTOS?

2/24/15:

A Time-Triggered Ethernet (TTE) Switch
The Time-Triggered Ethernet (TTE) Design

7. Describe what a sparse time base is and define the two key parameters it consists of.
8. How does a TTE switch handle an incoming Time-Triggered Ethernet message when a standard Ethernet message is already occupying the lane?
9. How is a fault-tolerant TTE configuration different from a standard TTE configuration? List the three extra components and their purpose.

2/26/15:

CPM: A Congestion Control Method for Interplanetary Network
Deep Space Autonomous Network Using Reverse Channel for Congestion Control

10. What are three problems found in deep space communication systems?
11. In a two-hop DSAN system, data is to be sent from Mars to Earth through an intermediate satellite. What is the purpose of the relay node?
12. Reverse Channel congestion control uses what method to prevent dropping packets?

The "Chimera": An Off-The-Shelf CPU/GPGPU/FPGA Hybrid Computing Platform
Fast and Flexible High-Level Synthesis from OpenCL using Reconfiguration Contexts

13. What are intermediate fabrics?
14. What are reconfiguration contexts?
15. What is the role of FPGA in the hybrid computing system used for astronomy?

3/10/15:

Virtualizing and Sharing Reconfigurable Resources in High-Performance Reconfigurable Computing Systems
Run-Time Resource Allocation for Simultaneous Multi-Tasking in Multi-Core Reconfigurable Processors

16. How is the execution cycle of High Performance Reconfigurable computer systems divided? List the 3 major divisions
17. Give a brief description of Single Program Multiple Data Model (SPMD)?
18. How do Multi-core reconfigurable processors exploit instruction level parallelism?

3/12/15:

Revolutionizing farming using Swarm Robotics

19. Briefly describe any 2 applications of Swarm Robotics.
20. In general, why is the Termite software used?
21. Give any 2 advantages of the system implemented in the paper

FPMR: MapReduce Framework on FPGA A Case Study of RankBoost Acceleration
A Reconfigurable MapReduce Accelerator for multi-core all-programmable SoCs

22. What are the advantages of on-chip dynamic scheduling?
23. In case of the FPMR framework used for the acceleration of RankBoost, what are the two factors that can cause a bottleneck in the speedup?
24. Explain any one advantage of MapReduce scratch-pad memory.

3/17/15:

Robustness of Evolvable Hardware in the Case of Fault and Environmental Change
Genetic Algorithms and Artificial Neural Networks to Combinational Circuit Generation on Reconfigurable Hardware

25. What are the three factors that can cause the circuit state to transform?
26. Why is a Mutation Rate of 100% the same as Mutation rate of 0%?
27. Name one advantage of Genetic Algorithms over Artificial Neural Networks for Reconfigurable Hardware?

3/19/15:

Reconfigurable Computing Middleware for Application Portability and Productivity
Programming Transparency and Portable Hardware Interfacing: Towards General-Purpose Reconfigurable Computing

28. What is a major obstacle for portability of hardware accelerators?
29. What is added benefit to having an abstracted virtualization layer between software and hardware threads?
30. RC Middleware abstracts away what aspect of FPGA development?

Design and Implementation of a Heterogeneous High-performance Computing Framework using Dynamic and Partial Reconfigurable FPGAs
Novo-G: At the Forefront of Scalable Reconfigurable Supercomputing
Maxwell – a 64 FPGA Supercomputer

31. How do the static logic and reconfigurable logic regions of the reconfigurable computing node communicate with each other?
32. In Maxwell, one of the requirements of target application is that “Computational Kernels should be small”, why?
33. Which factors will limit the performance of a FPGA based supercomputer, if it is not properly balanced?

3/24/15:

Reconfigurable Data Processing for Clouds

34. What is Cloud Computing?
35. Limiting Factors of using FPGS's in Cloud Computing??
36. What is a hypervisor? Briefly describe how the hypervisor works

Dynamic Power Consumption in Virtex™-II FPGA Family

37. Which portion of the FPGA has been identified as having the largest power inefficiency? Why?
38. Will static power for FPGAs be more or less important in future designs? Why?
39. 2. When analyzing the switching activity of various FPGA resources, one can observe that all resources follow the same general statistical behavior. Give two reasons why.

3/26/15:

Embedded Runtime Reconfigurable Nodes for Wireless Sensor Networks Applications

40. For the Cookie sensor network, what is the main purpose of the microprocessor?
41. How is the reconfiguration done and how is this method different from traditional reconfiguration methods?
42. If each node operates on AA batteries each having 1Ah and each node has a limited consumption of .02Ah. How many AA batteries are required at the node if the node operates on 3V and how many hours can the node last without the need for new batteries?

Comparing Performance and Energy Efficiency of FPGAs and GPUs for High Productivity Computing
GPU versus FPGA for high productivity computing

43. What is the difference between DDR and GDDR?
44. Why do GPUs show a fluctuating performance with varying batch size?
45. Why does GPU performance degrade for non-streaming data access?