4/2/15:

Dynamic Hardware/Software Partitioning: A First Approach
Exploration of Tasks Partitioning Between Hardware Software and Locality for a Wireless Camera Based Vision Sensor Node

1. What four main system components are used for the dynamic hardware/software partitioning system architecture used in this paper.
2. Which algorithm is used for routing and explain the routing algorithm's three main steps?
3. What are the three major components of a Vision Sensor Network (VSN)?

Low-Complex Dynamic Programming Algorithm For Hardware/Software Partitioning

4. What is a primary advantage and disadvantage of an entirely hardware-oriented architecture?
5. What is the main principle advantage behind dynamic programming?
6. In the PACE algorithm for hardware/software partitioning, what is being varied and what is the final target?

4/7/15:

Memory Management In Mobile Environment

7. There are three main concepts involved in the MMM architecture. LIST these three, and briefly describe ONE of them
8. What are two advantages of using the MMM architecture?
9. What does the MMM do in case of communication failure.

4/9/15:

Perceptron-based Coherence Predictors
AC/DC: An Adaptive Data Cache Prefetcher

10. What are coherence misses?
11. What is a perceptron in the context of computing and why was it chosen in the study to learn patterns?
12. What is cache pollution?

Modeling Communication in Cache-Coherent SMP Systems - A Case-Study with Xeon Phi
Analysis of MPI Shared-Memory Communication Performance from a Cache Coherence Perspective

13. What are two advantages of modeling shared-memory communication using micro memory benchmarks?
14. How do shared-memory MPI implementations handle large data transfers?
15. Explain the receiver driven approach for fast message broadcasting design model.

4/14/15:

The Salvage Cache: A Fault-Tolerant Cache Architecture For Next-Generation Memory Technologies

16. How does word disable (WDIS) work and what is its purpose
17. Briefly describe how a Salvage Cache works.
18. Why is salvage cache more effective when used with MRAM than SRAM?

FPGA Glitch Power Analysis and Reduction

19. What is a Glitch? Which type of circuits (synchronous or asynchronous) are affected by glitches in terms of correctness?
20. Why does the glitch reduction algorithm iterate through each LUT from shallower to deeper LUTs?
21. Why is combinational equivalence checking performed after glitch reduction step?

4/16/15:

Building A Swarm Of Robotic Bees

22. Briefly describe what swarm robotics is
23. What are the four main characteristics of swarm robotics?
24. What will happen to the system functionality if the coordinator node fails?

Physical Attack Protection with Human-Secure Virtualization in Data Centers
Virtualization of Hardware Resources as a Method of Power Savings in Data Center

25. What are two benefits for virtualization in datacenters.
26. What are two cyber defense mechanisms for data security.
27. What is virtualization?