Synthesis Study Guide

This is just for the synthesis portion of chapter 11. Other topics from the chapter will be on the test.

- synthesis levels (figure 11.3)
- Y-chart
- Logic synthesis
    - Point of it
    - Logic minimization
        - Point of it, not how to do it.
        - **Specifically, you do not need to know HOW to do it.**
        - Why is it hard
        - How do tools solve it if it is so hard
        - Difference between multilevel and two level logic minimization
            - A problem like on the homework
            - How do they trade off size vs. performance
    - FSM synthesis
        - What is it and what is the point.
        - State encoding
    - Technology mapping
        - What is it and how is it important
        - How can different technologies result in different circuits.
    - Why should logic synthesis be integrated with physical design? What has changed with decreasing feature size?
- Differences between logic, RT, behavioral, and system synthesis
- Temporal vs. spatial thinking

HFSM example

Here is a good example for splitting 1 FSM into 2 FSMs that is different that the fire model. You may see something like this on the test. You should also know the 2 main reasons for wanting to split FSMs.