11/3/11

SAFES architecture

- 1. How does using "a reconfigurable solution for security" expose the embedded system to a new security threat?
- 2. Why is it advantageous to use reconfigurable hardware to implement security primitives?

A System Architecture Exploration on the Configurable HW/SW Co-design for H.264 Video Decoder

3. Why are ASICs not suitable for H.264 decoding?

Hardware/software architecture of an algorithm for vision-based real-time vehicle detection in dark environments

4. For every potential pair of lights, the software part of the algorithm in the end tests several properties of the pairs, gives them a score out of 1 on every property and in the end calculates the total score for every pair. The score decides whether that pair are the actual taillights of a car or not. List four of the properties tested.

Bitmask Based Code Compression for Embedded Systems

- 5. Why is code compression critical in Embedded Systems.
- 6. Why are standard compression techniques not well suited for Embedded Systems?

11/8/11

Run-time reconfiguration for automatic hardware/software partitioning

7. How does parameterisable reconfiguration differ from traditional reconfiguration of FPGAs?

ROBTIC: On chip I-cache design for low power embedded systems

8. In what case does the ROBTIC cache controller have to go to the state "Cache Flush"?

11/10/11

A Study of the Speedups and Competitiveness of FPGA Soft Processor Cores using Dynamic Hardware/Software Partitioning

- 9. What are the 5 stages of the Warp Processor life cycle as presented in the presentation?
- 10. What are two disadvantages of soft processors as compared to hardwired processors?

Cost Efficient Memory Architecture Design of NAND Flash Memory Embedded Systems:

11. What are the advantages and disadvantages of using NAND Flash Memory Systems?

Design of NAND Flash Memory File System to improve boot time:

12. What are the 2 hardware constraints for write operations in NAND flash?

High Performance Cache Replacement Using Re-Reference Interval Prediction (RRIP)

13. List 2 benefits of RRIP for comparing to Least Recently Used(LRU) policy

11/15/11

Hiding cache miss penalty using priority based execution for embedded processors

14. Give two reasons why distinguishing between high and low priority instructions affords performance improvements?

Space Based Wireless Pico-Satellite Sensor Networks

15. How are Space Based Wireless Satellite Sensor Networks similar to regular wireless sensor networks?

11/17/11

Decoding-Aware Compression of FPGA Bitstream

16. In code compression, why is fixed-length code faster than variable-length code in for code compression?

An Efficient Code Compression Technique using Application-Aware Bitmask and Dictionary Selection Methods

17. What is the difference between Frequency based and Spanning based Dictionary selection scheme?

Power Optimization for Embedded System Idle Time In The Presence of Periodic Interrupt Services

- 18. The SA-1100 processor has three modes: run, sleep, and idle. How does system operation differ with respect to the clock signals and peripherals in these modes and what is the purpose for having multiple modes?
- 19. How does dynamic voltage/frequency scaling save power?

Power Dissipation in Cortical Implants

- 20. What is the main reason why an animal test is preferred over an in vitro test?
- 21. What are the dangers of having a cortical implant?

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Multi-Processor Embedded Systems

- 22. What is the difference between gated clocking and power gating.
- 23. What are three benefits for using divide-and-conquer automated logic design?

A Loop Accelerator for Low Power Embedded VLIW Processors

24. In a VLIW architecture, limiting the number of load/store ports limits the performance whereas a large number of ports degrades access time and power consumption. What are two methods for addressing this problem?