Low Power Embedded Systems in Bioimplants

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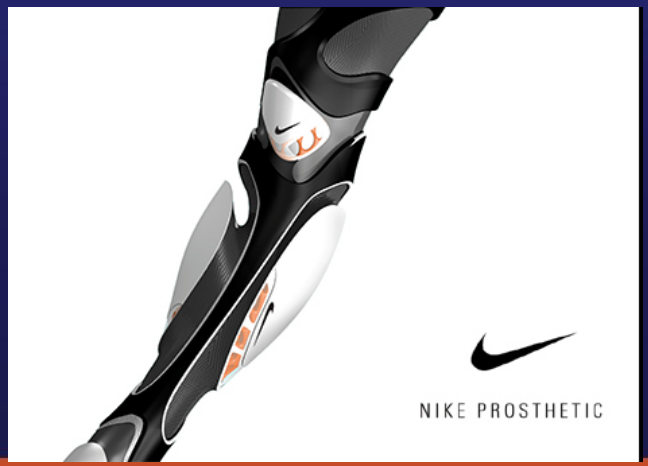
Why is it important?

- Lower limbs amputation is a major impairment.
- Prosthetic legs are passive devices, they do not do well in uneven terrain due to lack of torque at the artificial knee
- In order to develop better prosthetics we need to include embedded systems to make decisions
- Low power prolongs the longevity of the implant
- Thermally constrained



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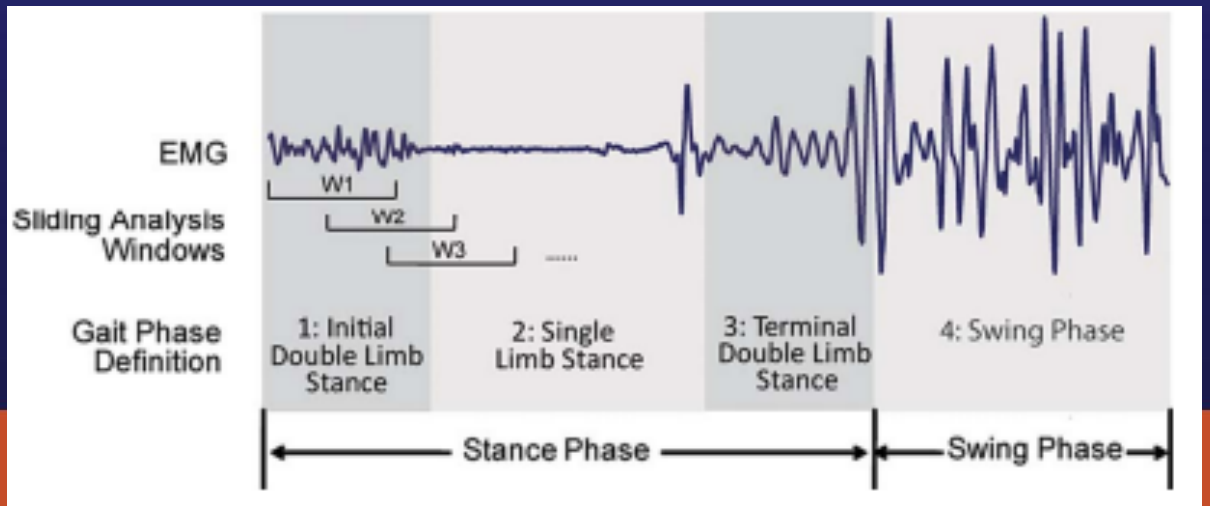
Promise of a Low Power Mobile CPU based Embedded System in Artificial Leg Control

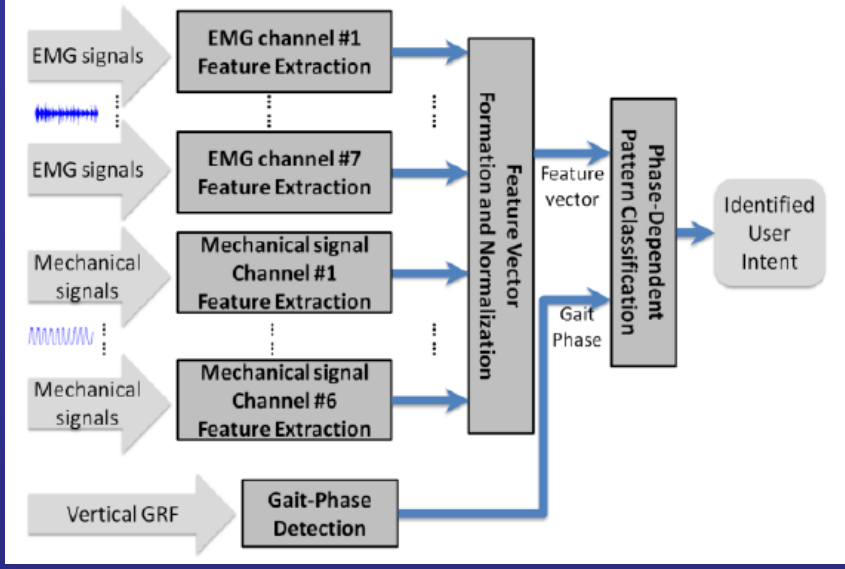
Hernandez, R.; Fan Zhang; Xiaorong Zhang; He Huang; Qing Yang, *Engineering in Medicine and Biology Society (EMBC), 2012 Annual International Conference of the IEEE* , vol., no., pp.5250,5253, Aug. 28 2012-Sept. 1 2012

Background

- Electromyographic Signals (EMG)
  - mean, number of slope sign changes, waveform length and number of zero crossings
- Mechanical Information
  - maximum, minimum and mean value of direction of force or moment
- Neuromuscular Mechanical Fusion



Algorithm



Neural-Machine Interface

- 6 classes
  - W, SA, SD, RA, RD , O
- 15 binary classifiers
- A voting strategy was used to make final decision, the mode with the most votes out of the 15 decisions was considered to be locomotion mode

TABLE I
SUMMARY OF DEMOGRAPHIC INFORMATION FOR FIVE SUBJECTS WITH TF AMPUTATIONS (TF01–TF05)

	Age	Weight (kg)	Height (cm)	Gender	Years post-amputation	Residual limb length ratio*	Prosthesis for daily use
TF01	51	80.3	177.8	M	32	82%	SNS Knee
TF02	56	75.2	173.4	M	38	62%	SNS Knee
TF03	26	53.4	160.2	F	25	40%	Total Knee
TF04	42	66.1	165.8	F	11	77%	C-Leg
TF05	57	75.8	175.3	M	31	51%	RHEO

*Residual limb length ratio: the ratio between the length of the residual limb (measured from the ischial tuberosity to the distal end of the residual limb) to the length of the non-impaired side (measured from the ischial tuberosity to the femoral epicondyle).

Algorithm

TABLE III
NUMBER OF MISSED TRANSITIONS AMONG ALL TESTED MODE TRANSITIONS

No. of Missed Transitions	TF01	TF02	TF03	TF04	TF05
SVM Fusion	0	0	0	0	0
SVM EMG	2	1	1	0	3
LDA Fusion	3	1	1	0	3

Note: The total number of tested task transitions was 75 for each subject.

TABLE IV
PREDICTION TIME OF MODE TRANSITIONS BEFORE THE CRITICAL EVENT

Unit: (ms)	W→SA	W→RA	SD→W	RD→W	W→O
SVM Fusion	420±175	390±140	652±143	355±231	301±156
SVM EMG	254±132	221±96	415±162	209±177	150±146
LDA Fusion	226±116	254±121	432±179	252±154	256±105

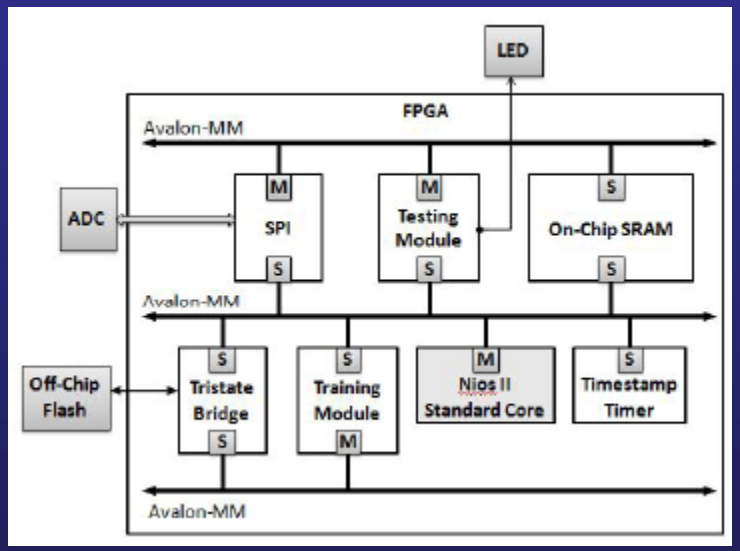
Note: W, SA, RA, SD, RD, and O denote level walking, stair ascent, ramp ascent, stair descent, ramp descent, and stepping over an obstacle, respectively.

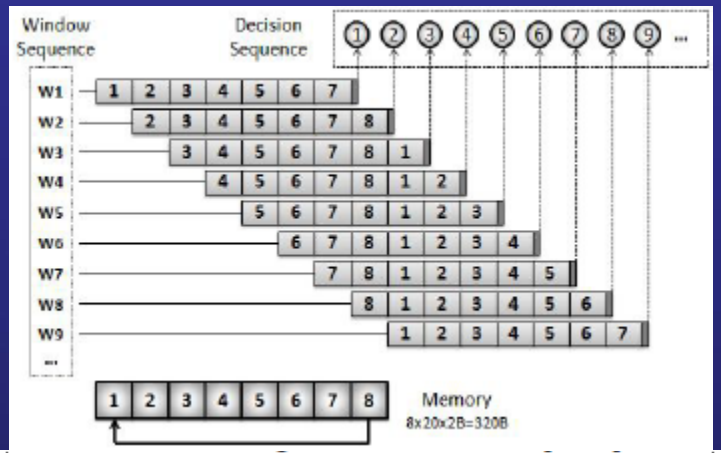
Phase-dependent PR

- LDA - linear discriminant analysis
- ANN - artificial neural networks
- SVM - support vectors machine
  - better accuracy
  - predicted task transition 50-200ms earlier before gait event
  - non-linear classifier might more accurately define boundaries among classes
  - SVM is more computationally efficient than ANN

FPGA

Altera Stratix II GX EP2S90



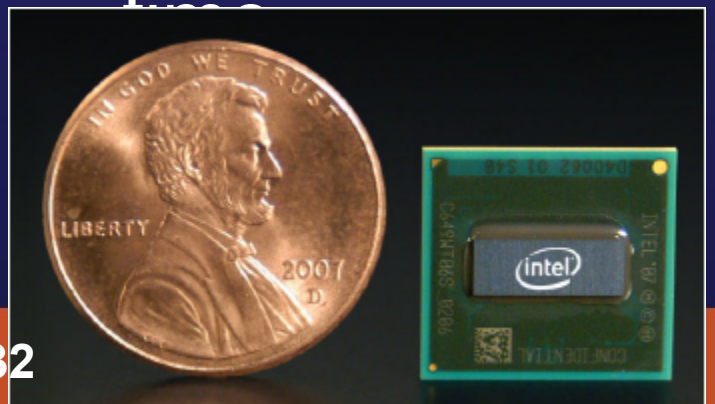


Window size	Software on PC	FPGA	Speedup
100	87.28 ms	28.93 ms	3.02
200	177.29 ms	56.94 ms	3.11
400	356.64 ms	112.94 ms	3.15

- Developing SVM algorithm on FPGA is challenging and time consuming. Limits ability to further optimize and develop NMI

Processor

- AxiomTek eBOX530-820-FL
  - thermally constrained and fanless embedded hardware.
- Intel Atom Processor Z530
  - 512k cache 1.6 Ghz
  - Hyper-Threading
    - OS and NMI application
- Code is written in C, lowers development time



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Results

1. Power consumed
   - AMD Turion 64x2 35 watts
   - FPGA 3.499 watts
   - Intel Atom 2.2 watts
2. Mean prediction time 0.8455 ms
   - Worse case 2.1265 ms
3. Better predictions results
4. Swing phase lower accuracies.
   - Swing phase longer, larger variations of EMG features and Little force/moment data
   - Can be improved by splitting swing into multiple phases

CLASSIFIER	MATLAB MODEL	EMBEDDED SW
PHASE 1	97.74%	98.33%
PHASE 2	96.72%	98.82%
PHASE 3	98.63%	98.67%
PHASE 4	95.18%	95.66%

Future work

- Combine with highly responsive data acquisition (DAQ) to lower sliding window to 10ms.
- Test the system on an amputee.

Issues with Research

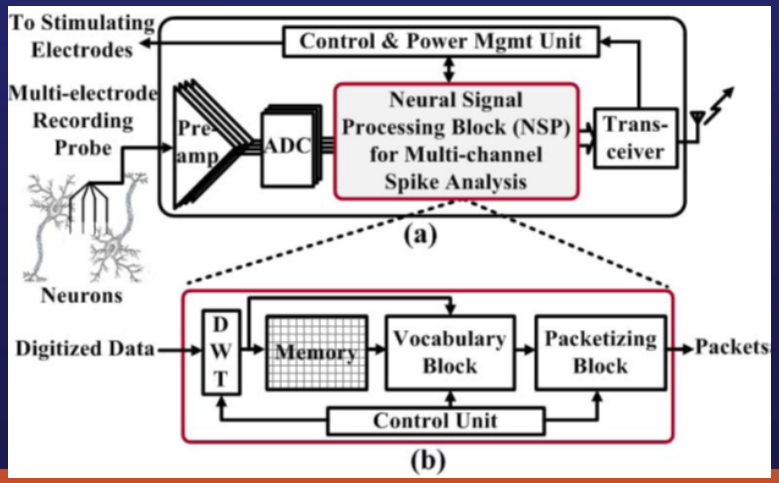
- What happens to double amputees?
- Did not try other processors
- Only about 40% of stratix was used, could have compared it to a smaller FPGA (Cyclone)

Ultralow-Power and Robust Embedded Memory for Bioimplantable Microsystems

Hashemian, M.S.; Bhunia, S., VLSI Design and 2013 12th International Conference on Embedded Systems (VLSID), 2013 26th International Conference on , vol., no., pp.66,71, 5-10 Jan. 2013

What?

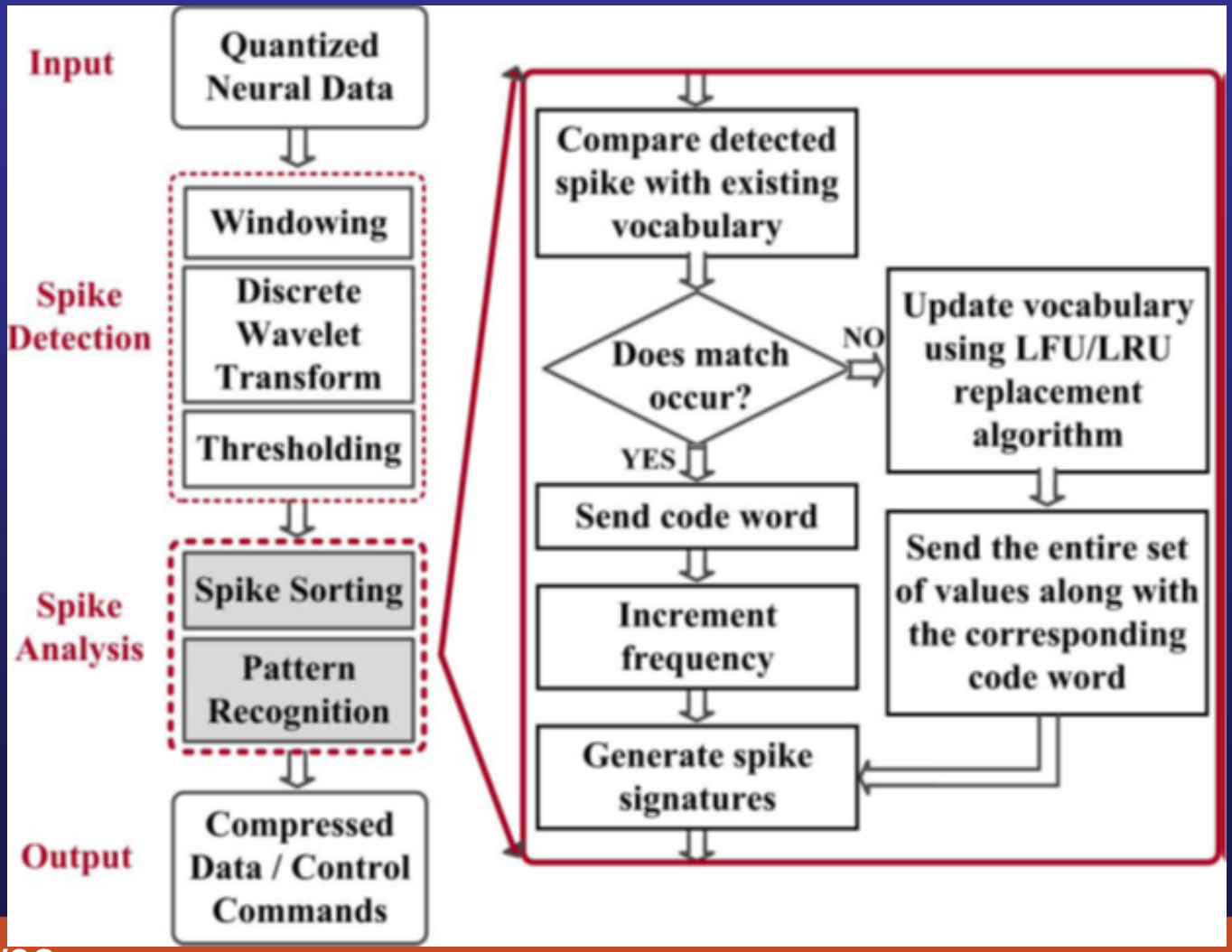
- Designing and testing different techniques to:
  - Lower power
  - Increase robustness
  - Decrease size
- of memory used in biologically implanted systems



Why?

- Sophisticated systems are acquiring more data
  - Amount of data is reaching limits of wireless transmission
  - Ex: 100 electrodes, 25kHz per channel, 10 bits of precision, 25Mbps
- Greater need to do on chip processing
  - Analysis, detection, and compression
- Environment limits device characteristics
  - Low power - Long battery life, low temp
  - Reliability - Not feasible to remove and repair
  - Size - Issues fitting large devices

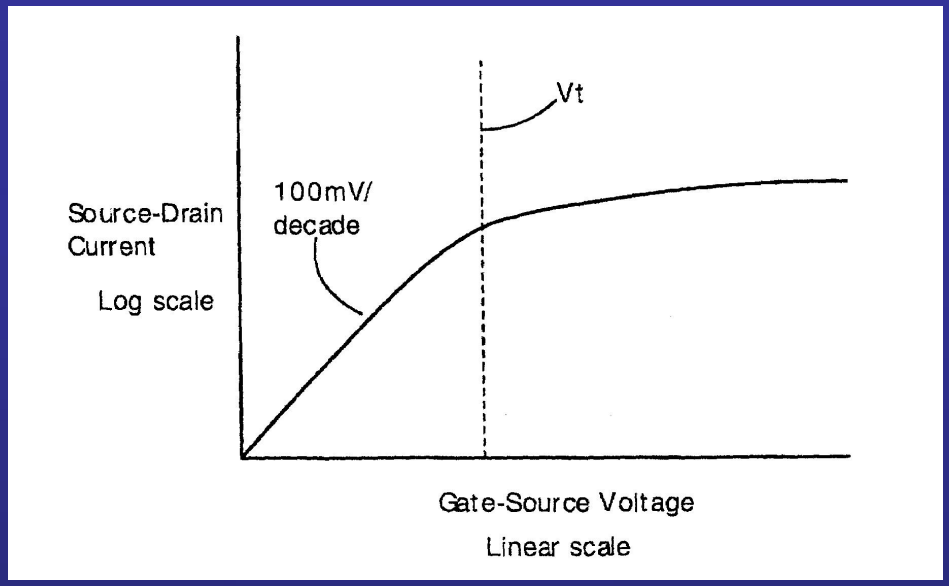
System Overview



Memory - Different Options

- A few options were considered
  - Array of Flip-flops
    - Pro: Extremely fast and easy to design
    - Con: Large area
  - Register File
    - Pro: Very Fast
    - Con: Power hungry, and design effort
  - SRAM
    - Pro: Fast, and small area
    - Con: Design effort

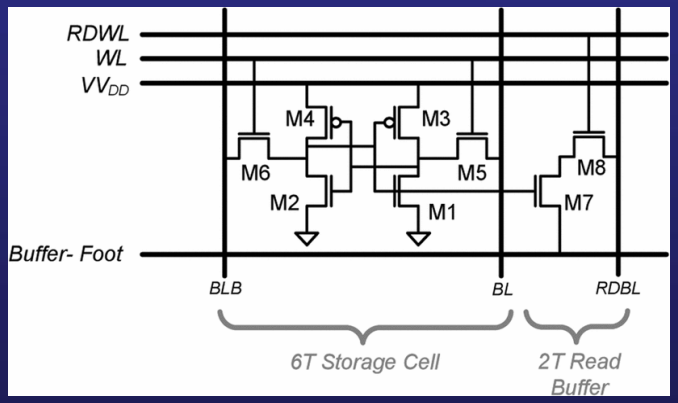
SRAM - Types



- Super-threshold
  - Fast
  - Well known - conventional 6T cell
  - Generally used for SRAMs
- Sub-threshold
  - Attractive with low power and low freq
  - Poor reliability and area overhead
  - Slow

SRAM - Sub-Threshold

- 8T and 10T cells considered
  - 8T denser
  - 10T reduces leakage
  - Both suffer from reliability issues



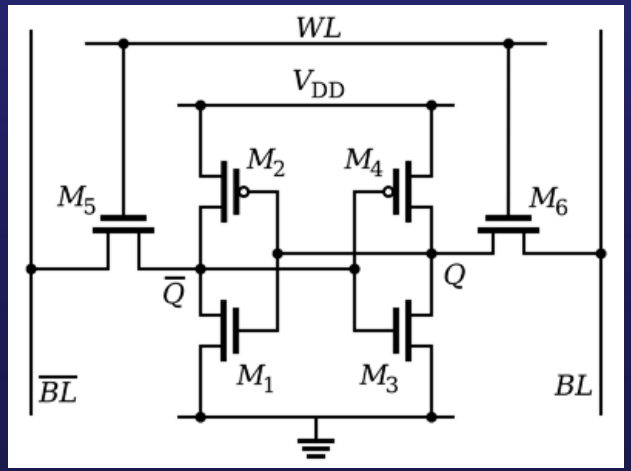
AREA, DELAY, ENERGY, AND NOISE-MARGIN FOR A 4X4 SRAM ARRAY IMPLEMENTED WITH 8T AND 10T SINGLE-ENDED CELLS

Cases	Area	Delay	Energy (zJ)			Noise Margin (mv)		
	μm^2	(ns)	dyn	leak	tot	Read	Write	Hold
8T	1.12	128.2	0.005	8.691	8.696	156	122	156
10T	1.44	200.4	0.02	6.576	6.596	156	122	156

- 8T selected due to higher density

SRAM - Super-Threshold

- 6T cell is:
  - Reliable
  - Fast
  - Dense
- Higher voltage increases power
  - Can be offset by supply gating



SRAM - Supply Gating

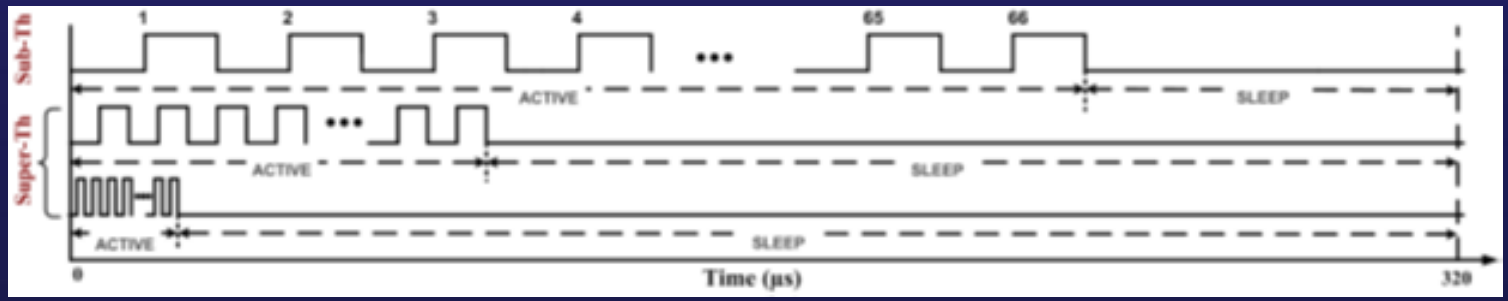
- Higher voltage cells have higher leakage power
  - Turn down supply voltage when not in use
  - Each row in memory is gated
  - Turn on row as its read
- Rows have a sleep transistor placed before GND
  - Transistor allows for a higher virtual GND during sleep
  - Effectively lowering supply voltage

Supply Gating - Considerations

- Sleep voltage needs to be set
  - Cell has a minimum data retention voltage
  - Sub-threshold cannot be gated
- Transition between GNDV and GND must be controlled
  - Cell's state could be disrupted
  - Adds delay and energy overhead for wake-up
    - 21% more time
    - 0.7% more energy

SRAM - The Better Choice

- Setup
  - 64 read operations + 1 write before next signal
    - 66 total cycles
  - 320us signal period
- Super-threshold
  - Compute quickly and sleep
- Sub-threshold
  - Computer slowly at lower voltage



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The Better Choice - Super-Threshold

- Increasing operating frequency
  - Increases dynamic power
  - Decreases time spent "active"
- Leakage power is frequency independent
- 620 MHz at 1V maximum

$$t_{clock} = max(t_{read}, t_{comp}, t_{write}) + t_{per}$$

TIMING PARAMETERS USED FOR DETERMINATION OF CLOCK CYCLE FOR A 'GATED' ARRAY

t_{read}(ns)	t_{write}(ns)	t_{comp}(ns)	t_{per}(ns)	t_{clock}(ns)
0.72	0.6	0.35	0.89	1.61

The Better Choice - Sub-Threshold

- Lower voltage
  - Decreases operating frequency
  - Decreases dynamic power
  - Decreases leakage power
  - Increases time required
- ~200kHz at 0.2V minimum

The Better Choice - Simulation

- 64x80 SRAM
  - Super-threshold at 1V, not gated
  - Sub-threshold at .4V
- 64 samples
  - 8 10 bit sample coefficients
  - Data acquired from sea-slug at 10kHz
  - 320us period

Simulation

- Super-threshold is
  - 611x faster than sub-threshold
  - 1.4x denser
  - More robust
- Sub-threshold
  - Less energy hungry

AREA, DELAY, ENERGY, AND NOISE-MARGIN FOR A 64X80 ARRAY REALIZED WITH THE CONVENTIONAL 6T SUPER-THRESHOLD AND THE SELECTED 8T SUB-THRESHOLD CELLS

Cases	Area	Delay	Energy (pJ)			Noise Margin (mv)		
	μm^2	(ns)	dyn	leak	tot	Read	Write	Hold
6T	256	0.37	40.48	69.61	110.09	209	420	383
8T	358.4	226	6.82	16.25	23.07	156	122	156

Simulation - Super-Threshold

- Gating vs non-gating
  - Significant energy reduction
    - 47%
    - Energy is still higher than sub-threshold, but other attribute compensate
  - Small area and noise increase
    - 3.6% and 2.4% respectively

AREA, DELAY, ENERGY, AND NOISE-MARGIN VALUES FOR A 64X80 ARRAY REALIZED WITH THE 'NOTGATED' AND 'GATED' SUPER-THRESHOLD CELLS

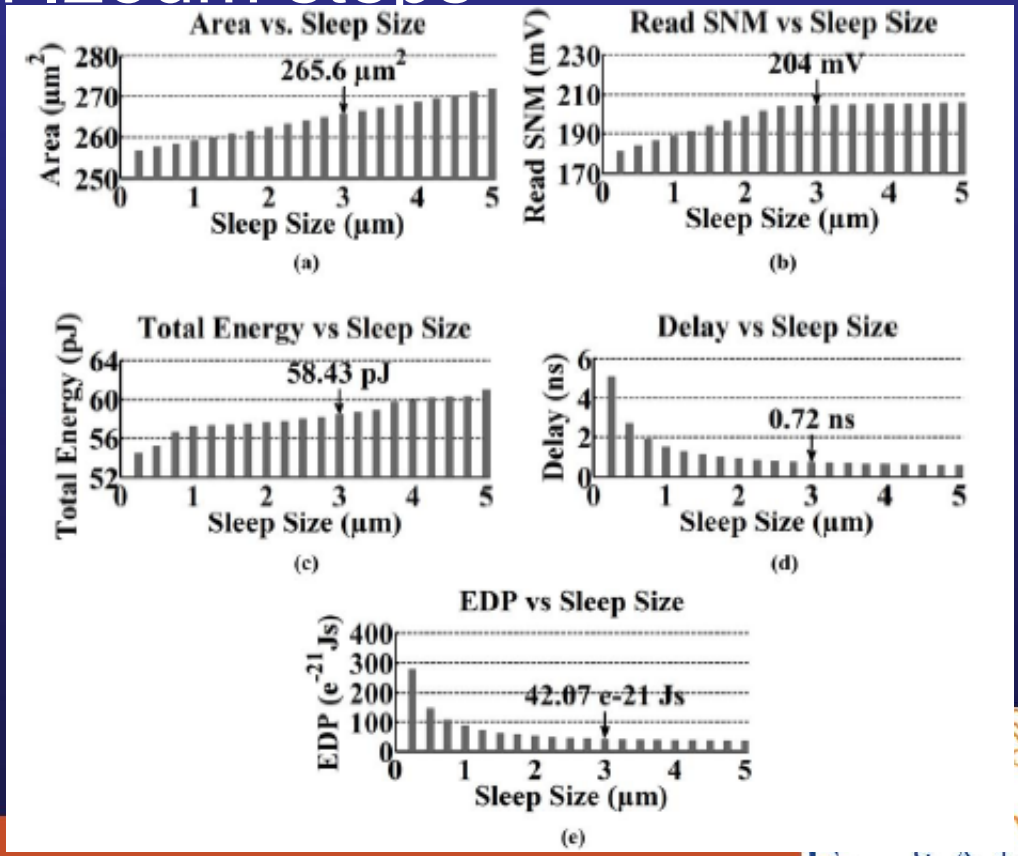
Cases	Area μm^2	Delay (ns)	Energy (pJ)			Noise Margin (mv)		
			dyn	leak	tot	Read	Write	Hold
NotGated Sup.th	256	0.37	40.48	69.61	110.09	209	420	383
Gated Sup.th	265.6	0.72	30.41	28.02	58.43	204	408	383

Super-Threshold - Tweaking

- Different attributes of the sleep transistor was changed and its effect on area, static noise margin (SNM), delay, energy, and energy-delay product (EDP) were measured

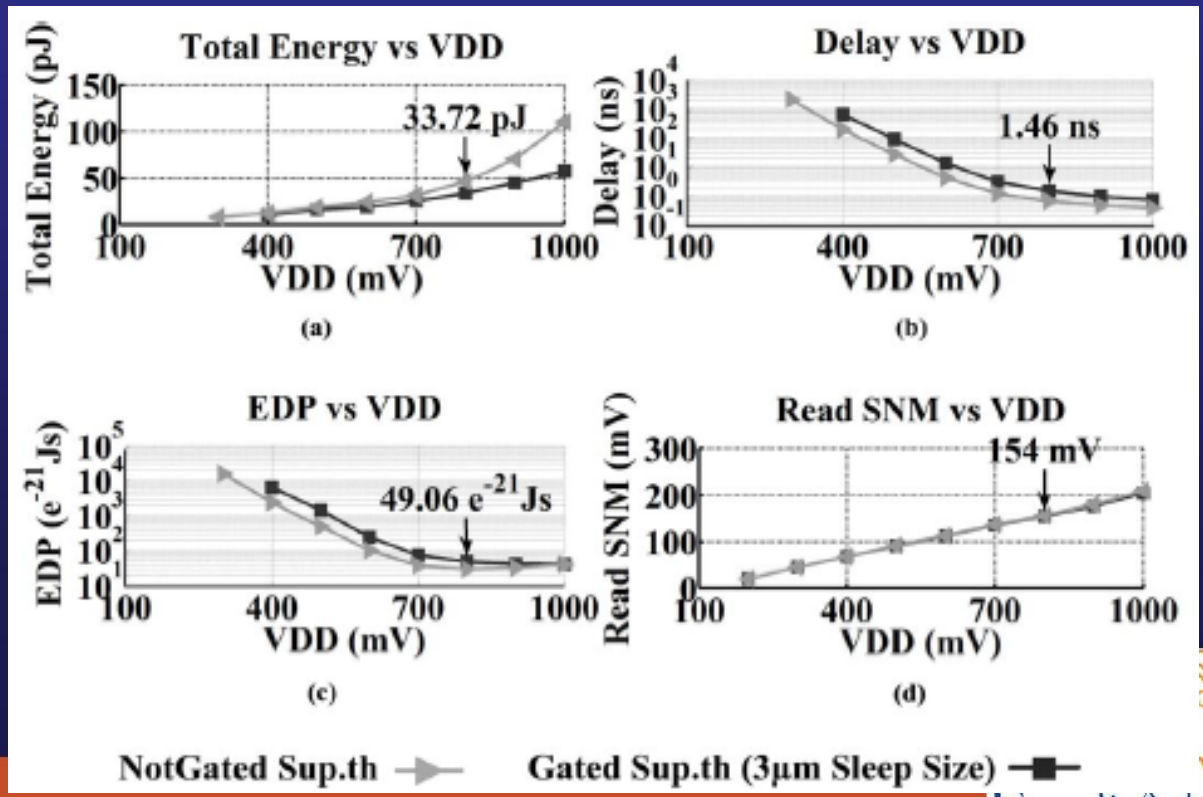
Tweaking - Size

- The size of the transistor was changed from 0.25um to 5um in .25um steps
- Optimal point was found to be at 3um



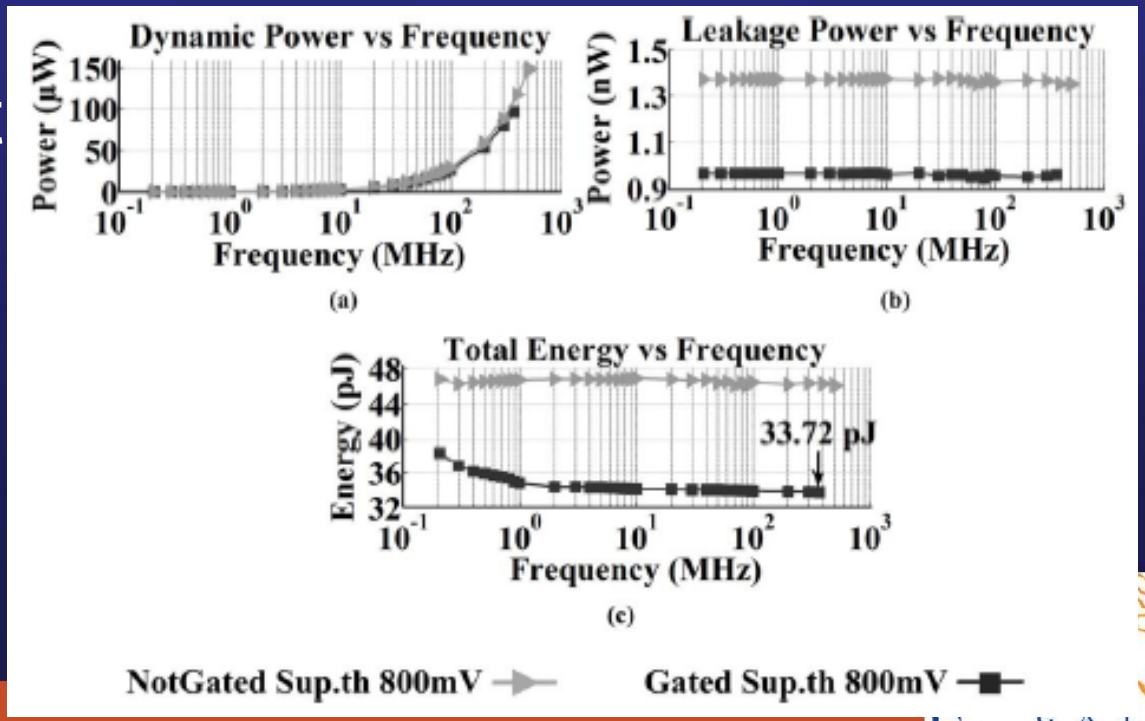
Tweaking - Voltage

- Vdd was adjusted from .3V to 1V
- Optimal was found to be 0.8V



Tweaking - Frequency

- Finally the operation frequency of the SRAM was adjusted from <10 Hz to 320MHz
- Optimal was found to be at the highest of 320MHz



Results

- The optimal configuration of SRAM was found to be
  - Super-threshold
  - Gated
  - 3um sleep transistor
  - at 0.8V
  - at 320MHz.
- This configuration is energy efficient, robust, and small

Future Work and Issues

- Future Work
  - Expanding concept to other subsystems
  - Expanding concept to other systems with high acquisition periods

- Issues
  - Authors do not go into detail about the modified SRAM cell.
  - No measure of reliability used