

1/10/13:

Design Framework for Partial Run-Time FPGA Reconfiguration

AND

Exploiting Partially Reconfigurable FPGAs for Situation-Based Reconfiguration in Wireless Sensor Networks

1. How does partial reconfiguration enable area savings?
2. How does partial reconfiguration enable cost savings?
3. How do single event upsets affect application functionality on FPGA?

1/15/13:

Dynamic Phase-based Tuning for Embedded Systems Using Phase Distance Mapping

4. How does phase-based tuning differ from application-based tuning? Why is phase-based tuning important, with respect to application requirements?
5. What is dynamic tuning? List three challenges with dynamic tuning?

1/22/13:

A Single-Pass Cache Simulation Methodology for Two-level Unified Caches

6. What is the definition of "cache tuning"?
7. Why does single-pass cache simulation speed up the simulation time as compared to iterative simulation?
8. Assuming that a configurable two-level exclusive cache consists of a level-one instruction cache, a level-one data cache, and a level-two unified cache. The sizes of level-one instruction and data caches can be configured to 2 KB, 4 KB, and 8 KB. The size of level-two unified cache can be configured to 16 KB, 32 KB, and 64 KB. All the three caches' associativities can be configured to direct-mapped, 2-way, and 4-way and the block sizes of all the three caches can be configured to 16 B, 32 B, and 64 B. If every cache parameter in the three caches can be configured independently, except for the block size (due to the exclusive cache requirement, the block size in all three caches need to be the same), what is the total number of configurations in the two-level exclusive cache design space?

1/24/13:

Assessing Performance Tradeoffs in Undersea Distributed Sensor Networks

9. What process is used to model detections by nodes in the undersea sensor network paper?
10. What are the two main parameters of the cost function in the undersea sensor network paper?

Space-Based Wireless Sensor Networks: Design Issues

11. Fill in the blank: The Flower satellite constellation scenario for Low Earth Orbit sensor networks displaces satellites equally along the _____ plane.
12. Fill in the blank: Distributed satellite communications use TCP for high-priority data and ___ for low-priority data.

ESPACENET - A Framework of Evolvable and Reconfigurable Sensor Networks for Aerospace-Based Monitoring and Diagnostics

13. In the ESPACENET framework the mother satellites are occasionally reconfigured for what purpose?
14. Name the three levels of hierarchy for ESPACENET satellites.

Development of a Satellite Sensor Network for Future Space Missions

15. Name two of the three technologies to be tested on for the Satellite Sensor Network space mission?
16. What are two major issues with wifi or 802.11 in an Inter-satellite link?

1/29/13:

Delay-Tolerant Networking: An Approach to Interplanetary Internet

17. What is a region in a delay tolerant network?
18. Why are standard internet protocols a poor choice for a delay tolerant network?
19. Why is a good delay tolerant networking architecture based on a postal model?

Reliability Options for Data Communications in the Future Deep-Space Missions

20. What organization is responsible to determining the standards in space communications?

21. What DTN protocol was implemented in the ISS?

1/30/13:

Harvesting Aware Power Management For Real Time Systems With Renewable Energy

22. List 3 main challenges in designing the power management for harvesting-aware real time system, in comparison with non-harvesting-aware real time systems.

23. What are the four main components of a harvesting-aware real time power management system?

Real-Time Scheduling With Regenerative Energy

24. Explain earliest deadline first algorithm.

25. Describe a situation where the Earliest Deadline First algorithm would fail when compared to the Lazy algorithm.

Communication Architectures for Dynamically Reconfigurable FPGA

26. Why do NoC-based networks show higher latency even though these networks are capable of supporting higher bandwidth?

27. Even though the results (table 3) show that DyNoC as better than CoNoChi, give a reason why CoNoChi is better than DyNoC?

A Light-Weight Network-On-Chip Architecture For Dynamically Reconfigurable Systems.

28. How does the placement of modules affect the reconfiguration capability?

29. What switching mechanism is used and briefly describe how it works.

2/5/13:

Tensilica – The Xtensa Processor Generator

(Note: The questions are only from the first 50 minute of the talk, the scheduled class time only)

30. The Xtensa Processor Generator automatically generates many tools and files for your system. What are two major outputs from the Xtensa Processor Generator?

31. Why is the Xtensa Processor highly competitive with all other microprocessors?

32. The Xtensa Processor has many configurable parameters/components. List 5.

02/07/13:

Pulling the Pieces Together at AFRL

33. Name three goals laid out in the Space Science and Technology Vector-2 plans.

34. What are two functions of xTEDS (XML Transducer Electronic Data Sheet)?

Development of the Malleable Signal Processor (MSP) for the Roadrunner On-Board Processing Experiment (ROPE) on the Tacsat-2 Spacecraft

35. Radiation-tolerant PROMs were used by the Malleable Signal Processor on the TacSat-2 to store FPGA _____ memory.

36. SRAM-based FPGAs are vulnerable to Single _____ Upsets caused by radiation in space.

Achieving Multipurpose Space Imaging with the ARTEMIS Reconfigurable Payload Processor

37. What function to the Mezzanine cards serve on the Responsive Avionics Reconfigurable Computer (RA-PCC)?

38. What are two methods employed by ARTEMIS to achieve fault tolerance.

Tactical Satellite 3 CDL Communications, a Communications Link for Mission Utility

39. What is the key advantage to the TacSat program?

40. What is two advantages of modifying airborne technology vs. creating something from scratch?