2/14/13:

An MDE Methodology for the Development of High-Integrity Real-Time Systems

1. What is a port cluster?
2. Which views in the architectural framework are platform specific?

An MDE-Based Approach For Reconfigurable DRE Systems

3. What is a mode transition?
4. What happens when an event is triggered in the metamode model

Worst-Case Execution Time Analysis for Parallel Run-Time Monitoring

5. What are the three challenges for adoption of Parallel Run Time Monitoring?
6. List three advantages of Parallel Monitoring

Leakage-Aware Dynamic Scheduling for Real Time Adaptive Applications on Mutliprocessor Systems

7. What is the impact on the leakage energy as the Vt reduces with technology?
8. What are Adaptable Applications? Provide two examples.

2/21/13:

Intermediate Fabrics: Virtual Architectures for Circuit Portability and Fast Placement and Routing

9. What are the three planes in an Intermediate Fabric and what is the basic purpose of each plane?
10. What is an Intermediate Fabric?

An FPGA-based Heterogeneous Coarse-Grained Dynamically Reconfigurable Architecture

11. What are the 3 components of the proposed CGRA?
12. What effect does adding an extra stage to an Omega network have on the block network?

Application Specific Customization And Scalability Of Soft Multiprocessors

13. What is a soft processor?
14. Why was the point-to-point topology better than the mesh topology?

PATS: Performance Aware Task Scheduler For Runtime Reconfigurable Processors

15. How does PATS differ from EDF?
16. Briefly describe how is the Reconfiguration sequence is determined?

2/26/13:

Questions for Efficient Search Space Exploration for HW-SW Partitioning

17. Explain how the DAG is used to facilitate HW-SW partitioning?
18. What does a vertex, edge, and edge weight represent in the DAG for this paper?

Questions for Integrating Physical Constraints in HW-SW Partitioning for Architectures with Partial Dynamic Reconfiguration.

19. What are the four key parameters of Priority function in heuristic approach?
20. Give one drawback and one advantage of ILP?

2/28/13:

Hardware/Software Optimization of Error Detection Implementation for Real time Embedded systems

21. What are the 2 main sources of overhead in EDI implementation, as discussed in the paper
22. Given a Process task graph, Overhead and mapping of tasks, what is the objective of EDI optimization?

3/14/13:

Dynamic Hardware/Software Partitioning: A First Approach

23. What is the function of the loop profiler? List two design restrictions that were imposed on the loop profiler.
24. List the three steps required for binary partitioning and list two advantages for partitioning at the binary level.

A Study of the Speedups and Competitiveness of FPGA Soft Processor Cores using Dynamic Hardware/Software Partitioning

25. List one advantage and one disadvantage for using softcore over hardcore processors.
26. Describe the basic idea behind warp processing?

Hybrid Cache Architecture Replacing SRAM Cache with Future Memory Technology

27. List four aspects that are considered in the cache model discussed in the paper?
28. List two features that make SRAM disadvantageous for future cache systems?

Bandwidth-Aware Reconfigurable Cache Design with Hybrid Memory Technologies

29. What kind of prediction mechanism is used for the prediction engine?
30. What are the two types of cache partitions at each cache level and how are they different from each other?

3/21/13:

On-chip Context Save and Restore of Hardware Tasks on Partially Reconfigurable FPGAs

31. List three drawbacks of prior work that on-chip software HTR addresses.
32. List two benefits HTR provides for multi-tasking systems.