3/26/13:

A Distributed BIST Control Scheme for Complex VLSI Devices

1. What is the main optimization focus of existing BIST scheduling approaches?
2. List 2 factors that are reduced when using a distributed architecture.
3. List the 4 BIST scheduling attributes.

A Hybrid BIST Architecture and its Optimization for SoC Testing

4. Why is testing in an SoC difficult?
5. List the 3 components of BIST?
   Test Pattern Generator (TPG)
6. While defining the test cost, what do CGEN & CMEM stand for?

4/2/13:

An Integrated Approach to Reducing Power Dissipation in Memory Hierarchies

7. What are two disadvantages of the Power-Aware DRAM Model (PADRAM) technique?
8. What are the four power modes for RDRAM?
9. How does the sequential first touch page placement policy work?

HitME: Low Power Hit MEmory Buffer for Embedded Systems

10. When does the HitME buffer updated and what is the motivation for this?
11. What system aspect is affected if there are too many offchip accesses?
12. How is the L1 cache size changed to limit the area increase when using a HitME buffer?

4/9/13:

Promise of a Low Power Mobile CPU based Embedded System in Artificial Leg Control

13. What are two key requirements for embedded systems in bio-implants?
14. What is a gait phase and list the four different phases?
15. What pattern recognition algorithm was used?

Ultralow-Power and Robust Embedded Memory for Bioimplantable Microsystems

16. What three attributes should the memory in Bioimplantable system have?
17. Why do implantable systems need memory?
18. What is the idea behind supply gating?

4/11/13:

FPGA Glitch Power Analysis and Reduction

19. What are the two categories of don't-cares and when does each category of don't-care occur?
20. What were the three steps performed on each lookup table (LUT) in the glitch reduction algorithm based on don't-cares?
21. What is vote bias?

GlitchLess: Dynamic Power Minimization in FPGAs through Edge Alignment and Glitch Filtering

22. What are the three parameters that define the programmable delay elements?
23. What is GlitchLess?
24. What is the main difference between the LUT Input scheme and the Gradual LUT input scheme?

4/16/13:

On-Chip Communication Buffer Architecture Optimization Considering Bus Width

25. How does the paper differ from the buffer optimizations proposed by previously researched methods?
26. What parameter describes the bus utilization? Give the formula.
27. What are the two conditions used to prune the architecture?

Communication Architecture Optimization: Making the Shortest Path Shorter in Regular Networks-on-Chip

28. What do large internode distances increase?
29. What do mesh networks lack?
30. What do repeaters help with?

4/18/13:

Scalable Vector Processors For Embedded Systems

31. What are the disadvantages of Superscalar and VLIW processors?
32. What are the three different types of vector memory access?
33. Why is the power consumption minimal in VIRAM?

Memory-Intensive Benchmarks: IRAM vs. Cache-Based Machines

34. What kind of memory access does the GUPS undertake?
35. What are the two important factors to be taken into account for the Histogram algorithm?
36. Why is the VIRAM disadvantageous for the SPMV benchmark?

Energy-Efficient Scheduling on Heterogenous Multicore Architectures
and
Energy-Efficient Signal Processing in Wearable Embedded Systems – An Optimal Feature Selection Approach

37. Name two application domains for wearable embedded systems.
38. Define relevance and redundancy, in the context of feature selection.
39. What is symmetric uncertainty?
40. How is energy usage predicted in this scheduling algorithm?
41. What is one reason statistical mapping would outperform our phase based approach?
42. Name one benefit of the phase based scheduling over other scheduling approaches for addressing power.