Name: _____

EEL 6935 – Embedded Systems Midterm 2 – Thursday, March 28, 2013- 100 points possible

Instructions:

- *Of the 11 questions, answer any 10. I will only grade the first 10 that you answer or if you answer more than 10, indicate the 10 that you want me to grade. There is no extra credit for answering additional questions.*
- *Answer each question in the context of the associated paper.*

An MDE Methodology for the Development of High-Integrity Real-Time Systems

1. What is a port cluster?
   A port cluster is a special UML composite port that aggregates elementary interaction points, called elementary ports

Worst-Case Execution Time Analysis for Parallel Run-Time Monitoring

2. List three advantages of Parallel Monitoring
   Enables many new capabilities (e.g., fine-grained memory protection, error bound checks, hardware errors)
   Protection against large class of software attacks
   High reduction (orders of tens of percent) in monitoring run time compared to single core monitoring

Intermediate Fabrics: Virtual Architectures for Circuit Portability and Fast Placement and Routing

3. What are the three planes in an Intermediate Fabric and what is the basic purpose of each plane?
   Data plane for basic computations
   Control plane provides primates for control logic and state machines
   Stream plane handles communication with eexternal memory

Application Specific Customization And Scalability Of Soft Multiprocessors

4. What is a soft processor?
   A microprocessor that is implemented entirely on an FPGA or Reconfigurable Fabric.

Efficient Search Space Exploration for HW-SW Partitioning

5. What does a vertex, edge, and edge weight represent in the DAG for this paper?
   Vertex represents the partitioning object.
   Edge represents a call or access to a callee object from the caller.
   Weights in an edge represent call count and HW-SW communication time.

Integrating Physical Constraints in HW-SW Partitioning for Architectures with Partial Dynamic Reconfiguration.

6. Give one drawback and one advantage of ILP?
   Long computation but optimal results

Hardware/Software Optimization of Error Detection Implementation for Real time Embedded systems

7. Given a Process task graph, Overhead and mapping of tasks, what is the objective of EDI optimization?
   To come up with an optimal fault tolerant worst case schedule length (WCSL)

Dynamic Hardware/Software Partitioning: A First Approach

8. List two advantages for partitioning at the binary level.
   Works with any software compiler and High level language

Hybrid Cache Architecture Replacing SRAM Cache with Future Memory Technology

9. List four aspects that are considered in the cache model discussed in the paper?
   - Miss rate
   - Memory access time (MAT)
   - Average memory access time (AMAT)
   - Power consumption

Bandwidth-Aware Reconfigurable Cache Design with Hybrid Memory Technologies

10. What kind of prediction mechanism is used for the prediction engine?
    - Statistical prediction or probability based prediction

On-chip Context Save and Restore of Hardware Tasks on Partially Reconfigurable FPGAs

11. List three drawbacks of prior work that on-chip software HTR addresses.
    Need for an external host
    Long external host communication times
    Lack of portability