An Integrated Development Toolset and Implementation Methodology for Partially Reconfigurable System-on-Chips

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Introduction

Motivations

- Scalable and flexible PR base architecture for rapid development of PR embedded systems
  - Virtual Architecture for Partially Reconfigurable Embedded Systems (VAPRES)
- Enabling hardware (HW) for research on intelligent HW resource management
  - Online HW module placement and scheduling
  - Dynamic migration of application tasks from software to HW

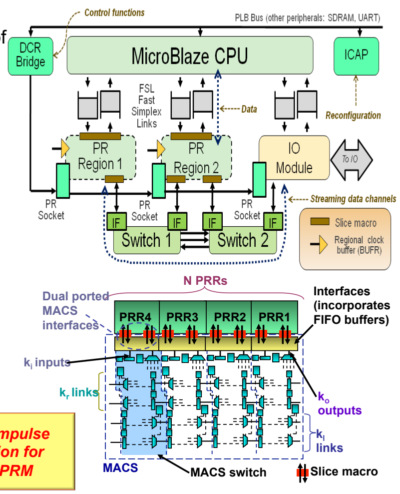
Highlights

- Integration of MACS inter-module communication architecture
- Integrated VAPRES System Builder (VSB) software
  - Develop both partially reconfigurable (PR) SoCs and applications
  - Support for both IOMs (static modules) and partially reconfigurable modules (PRMs)
  - Impulse C compatible hardware modules
- Implementation on both Virtex-4 and Virtex-5
  - Area profile, bitstream size, reconfiguration time

Architectural Support for Impulse C

VAPRES architecture

- Scalable and flexible architecture
  - Architectural parameters: number of partially reconfigurable regions (PRRs), FIFO depths, PRR width/ height, MACS
- Modules run in different clock domains
- Streaming communication
  - Asynchronous FSLs
  - Inter-module communication via MACS Network-on-chip (NOC)



Support for high-level synthesis (HLS) of PRMs using Impulse C

- Transparent integration of Impulse C hardware processes into VAPRES PRRs
  - Higher abstraction level reduces development time

```
//
// Prototype function declaration for the PR module.
//
void viaprestemplate(co_stream consumerfsl0, co_stream consumerfsl1,
co_stream producerfsl0, co_stream producerfsl1,
co_stream consumermacsleft, co_stream consumermacsright,
co_stream producermacsleft, co_stream producermacsright,
co_register producerleftaddress, co_register producerightaddress,
co_signal datain, co_signal dataout
)
```

Prototype Impulse C declaration for VAPRES PRM

Experimental Setup

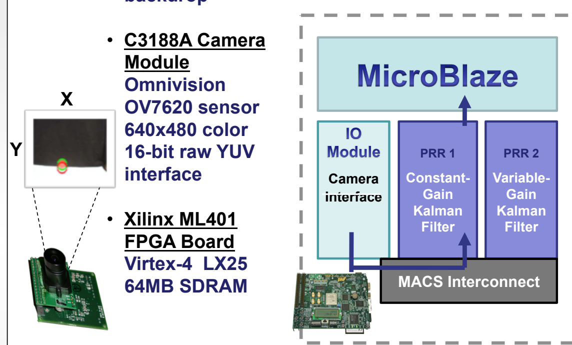
This experiment demonstrates adaptive target tracking of a ball using a camera and near-seamless filter swapping

Equipment

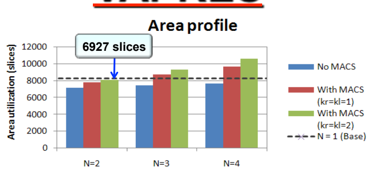
- **Target**
  Ball on cloth backdrop
- **C3188A Camera Module**
  Omnivision OV7620 sensor 640x480 color 16-bit raw YUV interface
- **Xilinx ML401 FPGA Board**
  Virtex-4 LX25 64MB SDRAM

VAPRES Setup

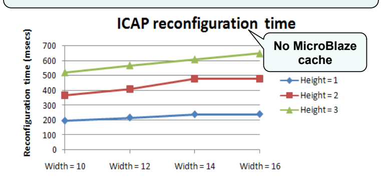
- **MACS Setup**
  3 switches
  1 channel left and right



VAPRES



- Average area increase per additional switch = 646.7 slices
- Average increase per channel at each switch = 302.4 slices



- Average ICAP bandwidth (with both MicroBlaze cache and barrel shifter disabled) = 0.63 MBps
- Average ICAP bandwidth (with both MicroBlaze cache and barrel shifter enabled) = 12.6 MBps

x20

VAPRES System Builder (VSB)

Motivations

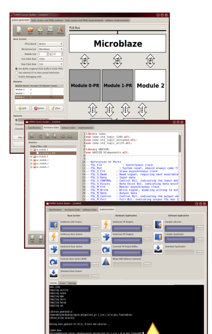
- Increased VAPRES portability to different FPGA families
- Integrated support for PRM development using Impulse C

Specifications

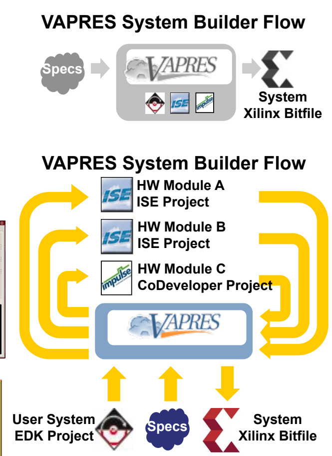
- Fully developed using Python/ GTK
- VSB functionality available for two Xilinx boards
  - ML401, OpenSPARC

Compatibility

- Enables management of VAPRES projects using first-party tools
  - Python API enables communication with ISE/ EDK/PlanAhead TCL shell
- VSB backend offers full compatibility with Xilinx DS 12.3



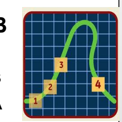
VAPRES System Builder (VSB) Snapshots



Adaptive Target Tracking

Application development using the VSB

- Kalman filters for target tracking
  - Tracks targets from noisy measurements
  - Highly parallel calculation ideal for FPGA



Specialized Kalman filters for different targets

Analysis	Basic (Variable-gain)	Constant-gain
Max Clock	156.2 MHz	71.4 MHz
Throughput	26 cycles / sample	3 cycles / sample
Power	80.92 mW	61.18 mW

Proposed algorithm

- Software application initially loads variable-gain Kalman filter inside a PRR
- Switches to constant-gain Kalman filter if filter gain does not change
  - Adaptive clock frequency keeps throughput constant
  - Software application adjusts PRR frequency