Introduction

- **Goals**
  - Efficient hardware resource management in partially reconfigurable (PR) system-on-chips (SoCs)
- **Motivations**
  - Enable multiple applications to concurrently execute on a PR SoC while meeting performance deadlines
- **Approach**
  - Leverage scalable and flexible base architecture
  - Virtual Architecture for Partially Reconfigurable Embedded Systems (VAPRES)
  - Implement dynamic resource manager (DRM) to orchestrate SoC hardware resource management
  - Improve hardware resource utilization and reduce reconfiguration time through run-time hardware adaptation

VAPRES Overview

- **VAPRES** is a parametric, scalable, and flexible architecture
  - Number of PR regions (PRRs), FIFO depths, PRR width & height, inter-PRR communication network
  - Inter-PRR communication using SCORES (a streaming-based dynamic inter-module communication architecture)
  - PR modules (PRMs) operate at different clock frequencies
  - Streaming communication with asynchronous FSLs

Dynamic Resource Manager

- **DRM** performs run-time hardware (HW) task scheduling and communication interface management
  - Caches HW modules inside PRRs
  - Enables HW reuse
  - Reduces wasted PR HW resources
  - Updates inter-PRR communication links for reconfigurable stream processing systems (RSPSs)
  - Eliminates HW relocation
  - Decreases overall reconfiguration time

RSPS Run-time Assembly

- **RSPS** netlists allow run-time assembly/ transformation of the inter-PRR data streams
  - Transformation done by dynamically updating SCORES communication channels
  - Allows PRMs to be seamlessly loaded/unloaded to PRRs without loss of processed data
  - DRM software modules execute inside the MicroBlaze CPU to ensure proper handoff