Formulation-level Design Space Exploration for Partially Reconfigurable FPGAs

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Introduction

Motivations

- Quantifying partial reconfiguration (PR) benefits is not straightforward
  - Many possible PR-architectures and architecture layouts on devices
  - Manual and tedious characterization, analysis, and evaluation process
  - Early design decision identification reduces design time effort
  - Formulation-level analysis affords short design exploration time

Approach

- PR design space exploration (DSE) in early application development phases
  - Evaluate device feasibility for PR-architecture(s) and layouts
  - Identify efficient PR-architecture layout(s) and device(s) for slower, more accurate implementation-level DSE
    - Reduces total accumulated implementation-level DSE time

Why architecture layout optimization?

- Increasing FPGA resource density
- Increasing resource type variation
- Improving PR region (PRR) resource utilization
- Improving implementation-level DSE output
- PR-architecture's suitability to a device

Requirements for layout optimization

- Application partition model
  - Static and PR modules (PRM)
  - Number of PRRs, mapping of PRMs to PRRs
- FPGA resource distribution model
  - Distribution of FPGA logic resources
  - Automatically generated for each device
- PR technology model
  - PR constraints
  - PR area overhead
- Optimization parameters
  - Internal and external fragmentation
  - Total area saving
- Pruned layout design space
  - Lowest fragmentation layouts
  - Other PR constraints

- Example design space for Xilinx V4 family
  - PRRs of 500~550 slices on biggest V4
    - Layout shape choices: 10,553; location choices: 27,196,103
    - Design space size: 287,000,470,000
- Pruned design space via formulation-level PR DSE (FoRSE)
  - 5 orders of magnitude reduction in design space
    - Layout choices: 52; location choices: 373,742
    - Design space size: 1,943,448

Formulation-level PR DSE (FoRSE)

python powered

FoRSE Phases

Phase - 1

Setup

- Basic
- Provides mathematical model for basic components (e.g., resource requirements, module, rectangular region on FPGA, etc.)
- Advanced
- Provides mathematical model for PR-architecture, device resource architecture, and PR-constraints

Phase - 2

Formalize

- Provides mathematical model for PR-floorplanning
- Defines potential PRR regions
- Incorporates vendor-provided PR- and tool-specific recommendations in model
- Defines all comparison metrics for PR-floorplan evaluation
- Considers area-centric metrics
- Designer designates competing metric pairs for PR-floorplan evaluation

Phase - 3

Execute

- Prepare
- Generates set of potential regions for each PRR based on PR-architecture
- Probe
- Generates set of PR-floorplans for a given device resource architecture
- Analyze
- Evaluates each designer-designated comparison metric for each PR-floorplan
- Iteratively executes prepare and probe for all target devices to generate Pareto-optimal sets of PR-floorplans and devices

Area Comparison Metric	Description
Internal utilization (IU)	Ratio of a PRR's mapped PRMs' resource requirements as compared to the PRR's available resources
External utilization (EU)	Ratio of the entire PR-architecture's resource requirements as compared to device's available resources
Expected resource saving (ES)	Percentage resource savings that application designer expects to gain by using a PR-architecture as compared to a non-PR-architecture
Actual resource saving (AS)	Percentage resource savings that application designer achieves by using a PR-architecture as compared to a non-PR-architecture
PR-overhead (PR_{ov})	Difference between expected and actual resource saving

FoRSE Experiments and Results

Input Parameters

- Sample PR-architecture [Table 1]
  - Estimated resource requirement for static and PRMs ($M_{x,y}$)
    - $M_{1,1}$, $M_{1,2}$, $M_{1,3}$ are mapped to PRR '1'
    - $M_{2,1}$ and $M_{2,2}$ are mapped to PRR '2'

***Table 1:* Sample PR-architecture**

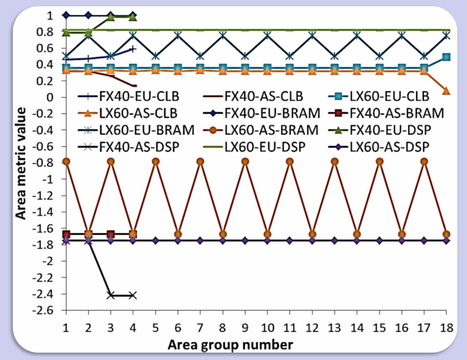
Resource type	Static	$M_{1,1}$	$M_{1,2}$	$M_{1,3}$	$M_{2,1}$	$M_{2,2}$	PRR '1'	PRR '2'
Slice	1365	277	224	195	611	772	277	772
BRAM	36	8	4	4	16	16	8	16
DSP	0	0	2	2	8	8	2	8

Evaluation Parameters

- External fragmentation and actual resource savings
  - Calculated individually for each resource type
- Evaluated all Virtex-4 FPGA devices
  - Estimated PRM resource requirements do not vary across devices in a family

Results and Observations

- Fast DSE (~15 seconds) with little designer effort
- PR-floorplan(s) may require more resources than non-PR-architecture
  - Depicted as resource's negative area metric values
  - Savings on one resource may adversely affect others
    - Reasons: device resource distribution, PR-constraints, and location, shape, and size of PRRs



PR-floorplans in the same *area group* have the same area metric values