Supplementary Material/Appendix for "High-Performance Energy-Efficient Multi-core Embedded Computing"

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Abstract—With Moore's law supplying billions of transistors on-chip, embedded systems are undergoing a transition from single-core to multi-core to exploit this high transistor density for high performance. Embedded systems differ from traditional high-performance supercomputers in that power is a first-order constraint for embedded systems whereas performance is the major benchmark for supercomputers. The increase in on-chip transistor density exacerbates power/thermal issues in embedded systems, which necessitates novel hardware/software power/thermal management techniques to meet the ever-increasing high-performance embedded computing demands in an energy-efficient manner. This paper outlines typical requirements of embedded applications and discusses state-of-the-art hardware/software high-performance energy-efficient embedded computing (HPEEC) techniques that help meeting these requirements. We also discuss modern multi-core processors that leverage these HPEEC techniques to deliver high performance per watt. Finally, we present design challenges and future research directions for HPEEC system development.

APPENDIX

HIGH-PERFORMANCE ENERGY-EFFICIENT MULTI-CORE PROCESSORS

This appendix provides additional description for some prominent multi-core processors and focus on their high-performance energy-efficient embedded computing (HPEEC) features.

ARM11 MPCore: The ARM11 MPCore processor features configurable level one caches, a fully coherent data cache, 1.3 GB/sec memory throughput from a single CPU, and vector floating point coprocessors. The ARM11 MPCore processor provides energy-efficiency via accurate branch and sub-routine return prediction (reduces the number of incorrect instruction fetches and decode operations), physically addressed caches (reduces the number of cache flushes and refills), and power and clock gating to disable inputs to idle functional blocks [1]. The ARM11 MPCore supports adaptive shutdown of idle processors to yield dynamic power consumption of 0.49 mW/MHz @130nm process. The ARM Intelligent Energy Manager (IEM) can dynamically predict the application performance and performs DVFS to reduce power consumption to 0.3 mW/MHz [2].

ARM Cortex A-9 MPCore: The ARM Cortex A-9 MPCore is a multi-issue out-of-order superscalar pipelined multi-core processor consisting of one to four Cortex-A9 processor cores grouped in a cluster and delivers a peak performance of 2.5 DMIPS/MHz [3]. The ARM Cortex A-9 MPCore features a snoop control unit (SCU) that ensures cache coherence within the Cortex-A9 processor cluster and a high-performance L2 cache controller that supports between 128K and 8M of L2 cache. The Cortex A-9 processor incorporates the ARM Thumb-2 technology that delivers the peak performance of traditional ARM code while providing up to a 30% instruction memory storage reduction. Each Cortex A-9 processor in the cluster can be in one of the following modes: *run mode* (the entire processor is clocked and powered-up), *standby mode* (the CPU clock is gated off and only the logic required to wake up the processor is active), *dormant mode* (everything except RAM arrays are powered off), and *shutdown* (everything is powered off) [4]. The ARM Cortex-A9 MPCore processor can support up to fourteen power domains: four Cortex-A9 processor power domains (one for each core), four Cortex-A9 processor data engines power domains (one for each core), four power domains (one for each of the Cortex-A9 processor caches and translation lookaside buffer (TLB) RAMs), one power domain for SCU duplicated tag RAMs, and one power domain for the remaining logic, private peripherals, and the SCU logic cells [4]. Typical ARM Cortex A-9 MPCore applications include high-performance networking and mobile communications.

MPC8572E PowerQUICC III: Freescale's PowerQUICC III integrated communications processor consist of two processor cores, enhanced peripherals, and a high-speed interconnect technology to match

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processor performance with I/O system throughput. The MPC8572E PowerQUICC III processor contains an application acceleration block that integrates four powerful engines: a table lookup unit (TLU) (performs complex table searches and header inspections), a pattern-matching engine (PME) (carriers out expression matching), a deflate engine (handles file decompression), and a security engine (accelerates cryptography-related operations) [5]. The processor uses DPM to minimize power consumption of idle blocks by putting idle blocks in one of the power saving modes (doze, nap, and sleep) [6]. Typical MPC8572E PowerQUICC III applications include multi-service routing and switching, unified threat management, firewall, and wireless infrastructure equipment (e.g., radio node controllers).

AMD Opteron Processor: The AMD Opteron is a dual-core processor where each core has a private L2 cache but shares an on-chip memory controller. The AMD Opteron 6100 series platform consists of 8 or 12 core AMD Opteron processors. The AMD Opteron's *Cool'n'Quiet* technology switches cores to low-power states when a temperature threshold is reached [7].

Intel Sandy Bridge Processor: The Sandy Bridge is Intel's second-generation quad-core processor that offers high sustained throughput for floating-point math, media processing applications, and data-parallel computation [8][9]. The processors's floating point unit supports the advanced vector extension (AVX) instruction set that allows vector processing of up to 256 bits in width. The processor leverages the hyper-threading technology that provides the OS with eight logical CPUs. Intel Sandy Bridge leverages Intel Turbo Boost Technology that allows processor cores and the built-in integrated graphics processor (IGP) to run faster than the base operating frequency if the processor is operating below power, current, and temperature specification limits [10]. The processor uses a ring-style interconnect between the cores offering a communication bandwidth up to 384 GB/s.

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